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A Review of Quantum-Dot Cellular Automata Based Adders

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Abstract

Quantum-Dot Cellular Automata (QCA) has been emerging as a new nanocomputing paradigm. QCA computing has many advantages like very high operating speed, extremely low energy dissipation, and very high device density. An adder is heart of arithmetic units of processors. So, many researchers have been working on design and implementation of reliable and robust QCA based adder circuit. This paper presents a comprehensive review of QCA based adder designs and implementations. Being an emerging future technology having potential of replacing CMOS technology, the paper comprehensively covers an introduction to QCA nanotechnology, QCA fundamentals, QCA technology developments, evolution of QCA adders, QCA full adder designs, performance metrics, and cost function computations for coplanar and multilayer QCA 1-bit full adders. The QCA adder circuits reported by various researchers have been compared in terms of adder type (coplanar or multilayer), basic full adder structure type, type and number of majority gates used, number of inverters, number of wire-crossovers, delay, and number of QCA cells. Also, the cost functions have been computed for both coplanar and multilayer QCA adders by giving higher priority to complexity.

Keywords*: Quantum cellular automata (QCA), Coplanar, Multilayer, Propagation delay, Cost function, majority gate, inverter*

1. Introduction

The continuous scaling down of feature size has pushed CMOS technology to approach its practical and theoretical limits [1]. Lot of research efforts at nanoscale are in progress to explore alternate viable technologies for future integrated circuits (ICs). QCA is emerging as a potential technology that could be used in future computing circuits/systems replacing existing Silicon technology. It provides a new computing and information transformation paradigm [2]. It is a transistor less technology that uses a square nanostructure called QCA cell comprising of 4 quantum dots [3]. Two free electrons are introduced in a four quantum dot based QCA cell which can tunnel amongst the quantum dots and take seat in any one of them. The two free electrons settle into two stable states within QCA cell that are used to encode two binary states in digital circuits. QCA cells are arranged in arrays for a particular computation and communicate with each other by Coulomb interactions. The alignment of electrons at edges of array provides the computational output. The alignment of polarizations in a QCA circuit is managed by applying an external clock and functions according to the rules of Boolean algebra [4].

This paper has been organized as follows: Section 2 presents fundamentals of QCA based computing. Section 3 discusses about QCA technology developments. Evolution of QCA adders is illustrated in Section 4. Section 5 covers QCA full adder designs and their

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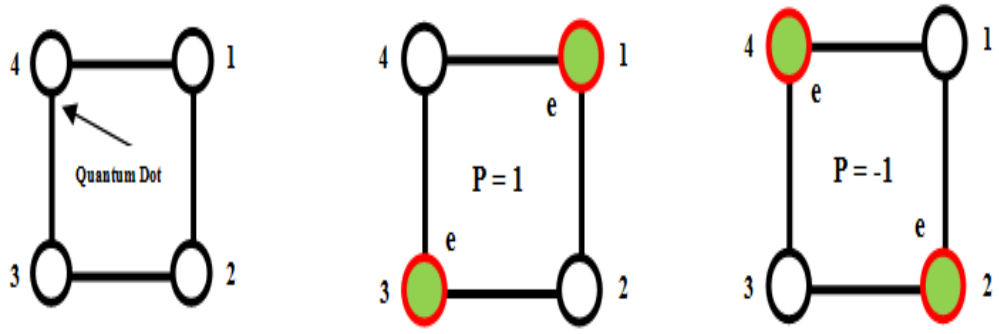
comparison in detail, Section 6 illustrates performance metrics of QCA adders, and Section 7 covers cost function computations for QCA adders. Conclusions are covered in Section 8.

2. QCA Fundamentals

2.1. QCA Review

The concept of Quantum cellular automata based digital signal processing was proposed by Lent and Tougaw [3] from Notre Dame University in 1993. The QCA cell comprises of a nanoscaled square nanostructure of 4 quantum dots. It is the most basic element used in forming arrays of cells for meaningful computations. The basic cell is depicted in Figure 1 (a). To make the QCA cell functional, two free electrons are introduced into the cell. The free electrons are allowed to tunnel within 4 quantum dots [4]. The quantum-mechanical tunneling causes electronic polarization of whole cell to settle into two stable ground states *'1'* and *'-1'*. These polarization states are used to encode two binary states logic '1' and '0' respectively. The binary state encoding is illustrated in Figure 1(b) and (c) respectively [5-7].



(a) (b) (c)

Figure 1. (a) Basic Four-dot QCA Cell, (b) Binary Logic '1' Encoding, and (c) Binary Logic '0' Encoding [3]

2.2. QCA Elementary Nanostructures

The Figure 2 illustrates a typical realization of binary wire in QCA technology. The polarization of the input cell in QCA wire causes the whole array to assume the same polarization due to coulombic interactions. There is no flow of current in QCA circuits only the electronic polarization changes; this results in extremely low power dissipation in QCA circuits/systems [4].

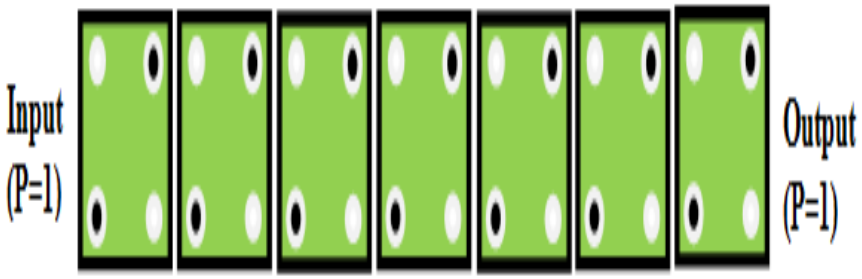


Figure 2. A Typical QCA Wire Implementation [4]

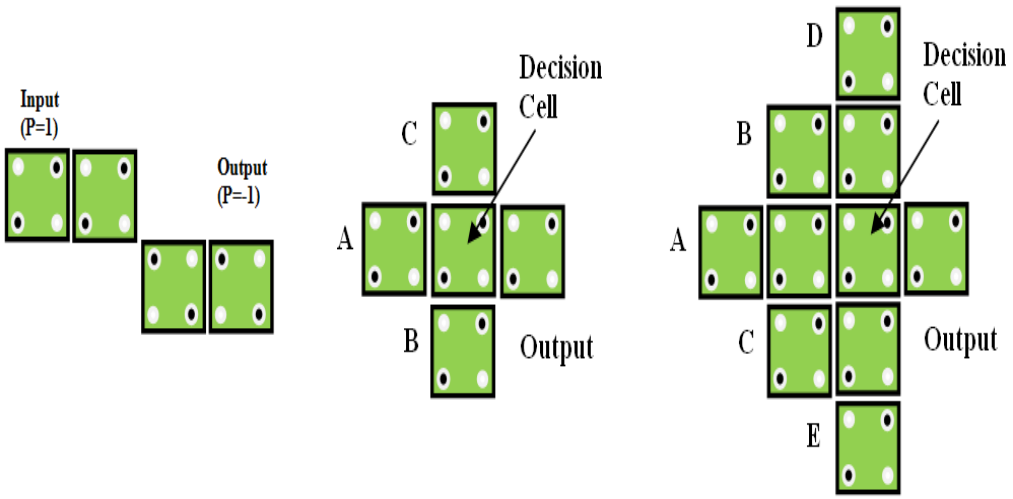


Figure 3. (a) A QCA Inverter Realization [5] (b) Basic 3-input QCA Majority Gate [5] and (c) A 5-input Majority Gate [8]

The Figure 3 (a) illustrates a mostly used QCA inverter implementation [5]. The fundamental computing gate in QCA is 3-input majority gate as depicted in Figure 3 (b). The middle cell in 3-input majority gate acquire a particular polarization as per majority of three inputs. The majority gate can be programmed to act as *AND* and *OR* gates by fixing polarization of any of 3 inputs to *'-1'* or *'1'* respectively. So, circuit/system designers can implement any Boolean function using majority and inverter gates [5-7] in QCA nanotechnology. The output of 3-input majority gate can be computed by equation (1).

$$MAJ\ (A, B, C) = AB + BC + AC \quad (1)$$

The 5-input majority gate is an emerging gate used in implementing complex QCA circuits/systems [8]. The Figure 3 (c) depicts a fundamental 5-input QCA based majority gate. The output of a 5-input QCA based majority gate can be computed using equation (2).

$$MAJ\ (A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (2)$$

2.3. QCA Clocking

The signal flow in QCA based circuits/systems is caused by application of appropriate clocking scheme. There are 4 different clock zones labeled as Clock-0 to Clock-3. Further, there are 4-phases in each clock zone namely *Switch, Hold, Release,* and *Relax*. There are 90^0 of phase-shift between 4 adjacent phases in a particular clock zone. The Figure 4 illustrates 4-phase clocking scheme. The clocking causes input polarization to flow in a pipelined manner from inputs to outputs [10].

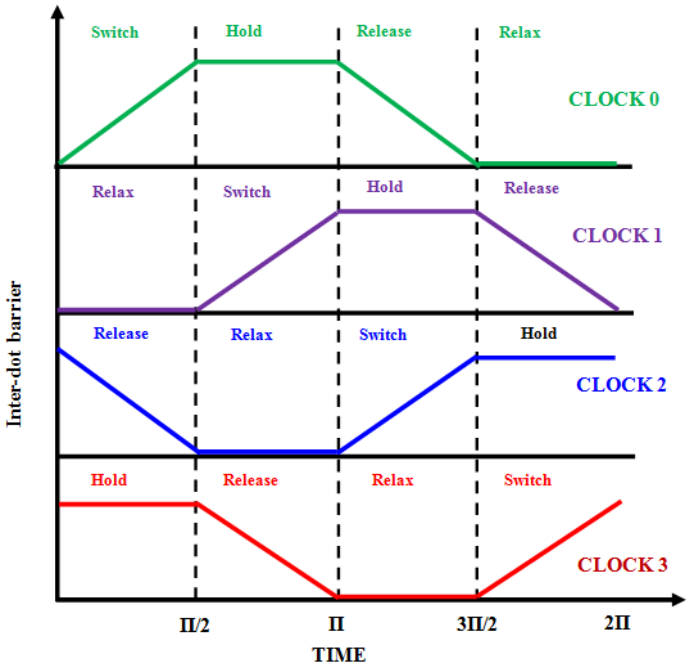


Figure 4. Clocking Flow in Different Clock Zones [10]

3. QCA Technology Developments

QCA nanotechnology is still under experimental research and not commercializes yet. There are experimental demonstrations of this technology by researchers in metal-island, molecular, semiconductor and magnetic QCA fabrication technologies. The first experimental demonstration of QCA technology was done in metal-island technology [11-12]. The four quantum dots were fabricated using Aluminum islands and connected among themselves using Aluminum oxide tunnel junctions and capacitors. The major limitation of this realization is that the metal island need to be kept at cryogenic temperatures for having electron switching as the size of quantum dot is in microns. Semiconductor QCA implementations [13-16] have been realized in advanced CMOS processes using GaAs/AlGaAs material system. However, existing CMOS processes did not reached a level where mass fabrication of QCA devices would become a reality. However, with continued feature size scaling as the size approaches a few nanometers, the semiconductor QCA devices would become able to operate at room temperature.

Molecular QCA are attracting lot of attention nowadays as they promise room temperature operation [16–19]. The molecules perform function of QCA cells and are attached to the substrate surface at adjacent sites. The redox sites act as quantum dots. The free electrons available in the molecule switch position between redox sites due to electrostatic interactions. The critical obstacles are selection of molecules, the design of appropriate clocking mechanism and how to interface molecules to real world. Magnetic QCA [20-22] works on the principle of interaction between magnetic nanoparticles. The magnetic moment of nanoparticles is used to represent two binary states in digital circuits. The moment is either parallel or anti-parallel in reference to the axis of the chain. The Magnetic QCA devices can work at room temperature in existing fabrication technology. The major limitation of magnetic QCA is limited speed of few hundred megahertz. The applications of magnetic QCA could be explored in low power areas where speed is not importance.

4. Evolution of QCA Adders

Adders are widely used in data processing and computing circuits such as Arithmetic Logic Unit (ALU) of processors. The performance of modern processors is decided by the speed, area, and power consumption of adders. Hence, design of a robust adder in QCA technology is basic necessity for a high performance arithmetic unit. Many researchers have introduced efficient and robust adder designs in QCA nanotechnology. Table 1 illustrates evolution of QCA adders over the period of time since their inception [5, 7, 23-59].

Table 1. Evolution of QCA Adders

Authors	Year	Research Brief
Tougaw and Lent [5]	1994	Demonstrated that QCA cells could be used to implement XOR gate and 1-bit full adder. The full adder design uses 5 majority gates and 3 inverters and 9 wire crossovers.
Lent and Tougaw [7]	1997	Realized an adiabatically pipelined QCA full adder circuit using new adiabatic switching paradigm allowing clocked control of QCA cell arrays.
Wang *et al.* [23]	2003	Presented a novel QCA adder design by minimizing number of majority gates, inverters and wire crossovers.
Rumi Zhang *et al.* [24]	2005	Proved that QCA based ripple-carry and bit-serial adders are faster than QCA based carry-look-ahead and carry-select adders.
H. Cho and E. Swartzlander [25]	2005	Designed 4, 16, and 64 bit carry lookahead adders in QCA and performed comparison with QCA ripple carry adders in terms of complexity, area, and delay. It was observed that carry lookahead adders offer modular designs.
H. Cho and E. Swartzlander [26]	2006	Discussed modular design of conditional sum adders (CSA) in QCA nanotechnology with different operand sizes and compared these designs with ripple carry adders and carry look-ahead adders.
K. Kim *et al.* [27]	2007	The failure analysis of QCA adders has been done and emphasized to exploit proper clocking schemes.
H. Cho and E. Swartzlander [28]	2007	QCA based Ripple carry, carry lookahead, and conditional sum adders are designed, analyzed, and compared with different operand sizes in terms of area, complexity and delay.
T. J. Dysart and P.M. Kogge [29]	2007	QCA designs of adders are analyzed based on probabilistic transfer matrices using triple modular redundancy (TMR).
E. Tabrizizadeh *et al.* [30]	2008	A new QCA serial adder has been designed which is delay-insensitive QCA. The registers are used to control the flow of information within the circuit modules.
I. Hänninen and J. Takala [31]	2008	Performed analysis of multi-bit ripple carry, conditional sum, and serial QCA adders.
I. Hänninen and J. Takala [32]	2008	Probabilistic analysis of a complete QCA multi-bit ripple carry adder (RCA) unit is performed and concluded that the reliability depends linearly on the failure rates of the macro level components.
H. Cho and E. Swartzlander [33]	2009	A new QCA based fast and efficient carry flow adder (CFA) is designed.

I. Hänninen and J. Takala [34]	2010	The analysis of logical bits lost in standard binary conditional sum, pipelined ripple carry, and carry look-ahead QCA adders have been performed.
I. Hänninen and J. Takala [35]	2010	A noise rejecting QCA full adder has been introduced for arithmetic units. Also designs of robust serial and pipelined ripple carry adders have been presented and functionally verified.
V. Pudi and K. Sridharan [36]	2011	Presented efficient QCA designs of Ladner–Fischer prefix and hybrid adders.
F. Bruschi *et al.* [37]	2011	Proposed QCA design of adder circuits by utilizing minority gates instead of majority gates resulting in significant reduction in number of cells required.
M. Gladshtein [38]	2011	Presented an algorithm for addition of two operands encoded by the Johnson–Mobius Code (JMC) to design a QCA serial decimal adder. The new adder is compared with parallel and conventional designs in terms of complexity, area, cost function and propagation delay.
W. Liu *et al.* [39]	2012	Reviewed several QCA adder designs and evaluated them based on newly proposed QCA performance metrics.
W. Liu *et al.* [40]	2012	Introduced two new cost-efficient binary-coded decimal (BCD) adders in QCA nanotechnology. The first adder is based on the carry flow adder (CFA) and employs a conventional correction method and the second adder utilizes the carry lookahead algorithm. Both adders outperform previous adders in terms of delay and overall cost.
V. Pudi and K. Sridharan [41]	2012	Introduced new concepts for majority logic and utilized them to design efficient QCA ripple carry adder (RCA) and various prefix adders. The number of majority gates employed for n-bit Kogge–Stone, RCA, Ladner–Fischer, Brent–Kung and Han–Carlson adders are also computed.
S. Perri *et al.* [42]	2012	The properties of auxiliary propagate and generates signals have been explored to minimize the addition time and number of majority gates required for QCA adders. Also introduced three new formulations of basic logic equations used in the designs of fast binary adders.
V. Pudi and K. Sridharan [43]	2012	Introduced two new decomposition theorems helpful in reducing delay in multi-bit QCA adders.
M. Gladshtein [44]	2013	Demonstrated two original QCA serial decimal adder/subtractor designs using a delay element implemented by short length of QCA wire as a function element avoiding traditional parallel Boolean logic processing.
A. Thamos and H. T. Vergos [45]	2013	Presented QCA implementations of parallel prefix Ling-Carry adders that use a Ladner-Fischer parallel-prefix algorithm for carry computation.
K. A. Escobar and R. P Ribas [46]	2013	Presented the design of a complex adder using the parallel prefix addition algorithms.
Bibhash Sen *et al.* [47]	2013	A new multilayer QCA full adder design implemented using five-input majority gate. The new design is analyzed by implementing ripple carry adders of different operand sizes and compared with other adder designs.

M. Kianpour *et al.* [48]	2014	Successfully designed, implemented and simulated a new QCA full adder having minimum delay, area and complexities.
E. McLarnon *et al.* [49]	2014	A bit erasure analysis of carry flow, Brent-Kung and Ladner-Fischer adders is presented.
M. Gladshtein [50]	2014	A new technique 'delay-based processing-in-wire' is proposed for designing QCA 1-bit and multi-bit serial decimal adders based on serial decimal data storage-transfer-processing and Johnson-Mobius encoding.
S. Perri *et al.* [51]	2014	A new QCA adder is introduced which outperforms all existing adders and exhibits best area-delay tradeoff.
D. Kunalan *et al.* [52]	2014	A QCA based 4-bit ripple carry adder is introduced using the new reversible Feynman and Toffoli gates.
Z. Mohammadi *et al.* [53]	2014	Conventional reversible Toffoli and Fredkin gates based full adder is designed and investigated.
M. Hayati and A. Reza [54]	2014	Optimized one-bit full adder, full subtractor, full adder/ full subtractor and a 4-bit carry flow adder in QCA nanotechnology. Also the cell-missing defects are investigated for defect characterization and testing of the proposed full adder.
D. Abedi *et al.* [55]	2015	The new QCA adder has been designed using non-adjacent clock zones (shifted by 180^o) for the two crossing wires. This results in reduction of QCA cell count and area consumption.
R. Farazkish [56]	2015	A novel QCA fault-tolerant full-adder has been proposed which is significantly more robust to single or multi-faults in missing cells, misalignment cells and dislocation cells.
A. Roohi *et al.* [57]	2015	Introduced an efficient layered fault-tolerant design for 1-bit full adder.
S. Hashemi and K. Navi [58]	2015	Introduced a novel robust QCA full-adder implemented using an efficient five-input majority gate. It is then used to realize ripple carry adders with different operand sizes.
A. N. Bahar and S. Waheed [59]	2016	Proposed a new flexible 5-input majority gate and a new efficient QCA based full-adder design. The new design offers significant improvement in comparison to the previous designs in terms of covered area and number of QCA cells.
G. Singh *et al.* [62]	2016	Introduced a new novel robust XOR gate in QCA technology which can be employed in arithmetic and communication circuits/systems.
G. Singh *et al.* [63]	2017	Presented design and performance analysis of a new efficient coplanar quantum-dot cellular automata adder and also carried out its energy dissipation analysis.

5. QCA Full Adder Designs

A full adder has 3 inputs and two outputs *'Sum'* and *'C_{out}'*. The *'A'*, *'B'*, and *'C_{in}'* are inputs as shown in Figure 5. The generalized Boolean equations for *'Sum'* and *'C_{out}'* are given in equations (3) and (4) respectively:

$$\text{Sum} = (\text{A}) \textit{ xor } (\text{B}) \textit{ xor } (\text{C}_{\text{in}}) \quad (3)$$

$$\text{C}_{\text{out}} = (\text{A}) \textit{ and } (\text{B}) \textit{ or } (\text{B}) \textit{ and } (\text{C}_{in}) \textit{ or } (\text{C}_{\text{in}}) \textit{ and } (\text{A}) \quad (4)$$

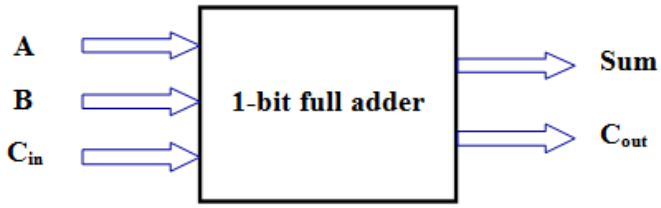


Figure 5. Block Diagram of 1-bit Full Adder

QCA adders are classified mainly into two major categories depending on the type of wire crossover method used in the design:

a) Coplanar Adders: All QCA cells in design are arranged in only one layer and employs normal and rotated cells (45º) for wire crossover or no wire crossover at all. However, in coplanar wire crossover is prone to thermal defects. So, it should be better if there is no wire-crossover in designed QCA circuits as it enhances reliability of the circuit. Clock zone based crossover is the most recent, robust, fast, and low cost coplanar wire crossover technique. It basically uses two clock zones separated by 180 degree to cross two wires. Delay optimization become difficult in this technique as the complexity of the circuit increases.

b) Multilayer Adders: It employs multiple layers of cells similar to many metal layers used in integrated circuits (ICs). The major advantages are effective crossing of signals and lesser area required than coplanar QCA circuits. However, it still lacks physical implementation and moreover the fabrication cost is expected to increase by threefold.

4.1. Coplanar Full Adders

Tougaw and Lent Adder

The first design for a 1-bit QCA full adder was proposed by Tougaw and Lent [5]. It uses 5 majority gates and 3 inverters. The *'Sum'* and *'C_{out}'* outputs are calculated in terms of majority gates and inversion operation as described by equations (5) and (6) below:

$$Sum = M3(M3(\overline{A}, B, C_{in}), M3(A, \overline{B}, C_{in}), M3(A, B, \overline{C}_{in}) \quad (5)$$

$$C_{out} = M3(A, B, C_{in}) \quad (6)$$

The number of majority logic gates, inverters and wire crossovers required are *5n*, *3n* and *9n* for an n-bit Tougaw and Lent full adder. The delay is *n + 1/4* clock cycles for n-bit adder. The major limitation of this adder is high number of wire crossovers and poor clocking scheme. Also it uses 45º rotated QCA cell for wire crossovers which provide poor coupling. The Figure 6 (a) shows the schematic diagram of 1-bit Tougaw and Lent full adder.

Wang Adder

Wang used majority logic reduction methods to optimize and simplify the layout of Tougaw and Lent full adder [23]. The n-bit Wang adder comprises of only *3n* majority gates, *2n* inverters and *6n* wire crossovers. The complexity is reduced; however, the propagation delay is equal to Tougaw and Lent adder. The delay of n-bit Wang adder *n +1/4* clock cycles. The output carry computation is similar to Tougaw adder. The *'Sum'* is calculated in terms of majority gates and inversion operation as described by equation (7).

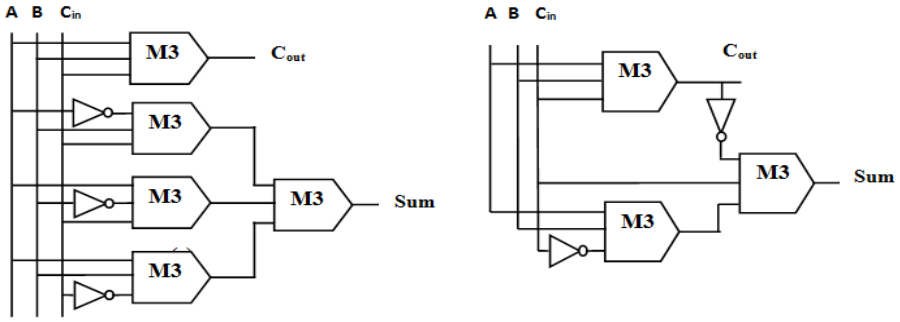
$$Sum = M3(\overline{C}_{out}, C_{in}, M3(A, B, \overline{C}_{in}) \quad (7)$$

The major advantage of this adder is efficient clocking scheme which minimizes crosstalk between inputs. The Figure 6 (b) shows the schematic diagram of 1-bit Wang full adder.

D. Abedi Adder

This QCA adder design employs clocking mechanism for wire crossovers [55]. It uses two non-adjacent clock zones shifted by 180^o for crossing two wires. This results in the design of QCA full adder with significant reduction in QCA cell count and area. This adder structure uses *3n* majority gates, *2n* inverters and no wire crossover for an n-bit adder. The 'Sum' function for this adder is computed using equation (8) below.

$$Sum = M3(\overline{C}_{out}, M3(A, B, \overline{C}_{in}), \overline{C}_{in}) \tag{8}$$



(a) (b)

Figure 6. Schematic Diagrams of (a) 1-bit Tougaw and Lent Full Adder [5] and (b) 1-bit Wang Full Adder [23]

Hanninen and Takala Adder

This QCA adder is optimized logical layout of Wang's adder [31]. The optimization has been performed by efficiently rearranging the clocking zones to realize a robust adder design. It uses only *3n*, *2n*, and *3n* number of majority gates, inverters and wire crossovers for an n-bit Hanninen and Takala adder. However, the delay of this adder has degraded which is *n+1* clock cycles for an n-bit adder.

M. R. Azghadi adder

This QCA adder design employs 5-input majority gate along with a 3-input majority gate and an inverter to realize a 1-bit full adder [60]. The use of 5-input majority gate facilitates simplifying complex logical functions and achieve improved results. This also helps in reducing gate counts required to implement digital functions. The Figure 7 shows the schematic diagram of 1-bit QCA Azghadi full adder.

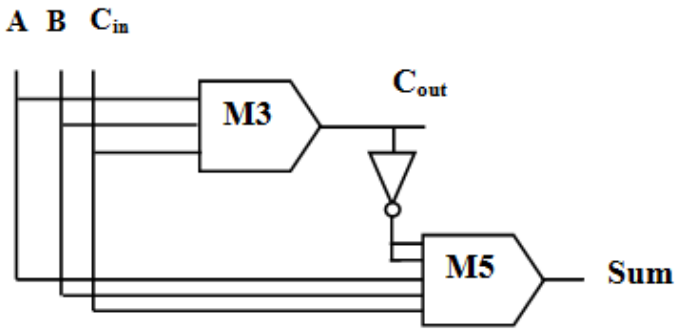


Figure 7. Schematic of 1-bit QCA Azghadi Full Adder [60]

4.2 Multi-Layer Adders

Zhang Adder

This QCA adder is just multi-layer implementation of Wang's adder. It utilizes the same addition algorithm [24]. It uses *3n* majority gates, *2n* inverters and *3n* multilayer wire crossovers for an n-bit adder. The delay is *n* clock cycle which is less than Wang's adder. The cost of coplanar and multi-layer crossings is quite different.

Cho Adder

A new optimized carry flow adder was introduced by Cho [25]. The path from carry in to carry out make use of one majority gate. This adder uses only one clocking zone delay per bit which considerably minimizes delay for large-size adders. It uses *3n* majority gates, *2n* inverters and *2n* crossovers respectively. The delay of an n-bit Cho adder is $\frac{n+2}{4}$.

Pudi Adder

Pudi proposed QCA based Brent-Kung adder design [36]. It is basically a parallel prefix adder. Majority logic reduction techniques have been used to improve performance in terms of delay for large-bit adders. This adder structure minimizes carry computation to a prefix computation. The output *'Sum'* and *'C_{out}'* of Pudi's adder are calculated by equations (9) and (10) respectively.

$$Sum = M3(\overline{C}_{out}, M3(g, p, \overline{C}_{out}), C_{in}) \tag{9}$$

$$C_{out} = M3(g, p, C_{in}) \tag{10}$$

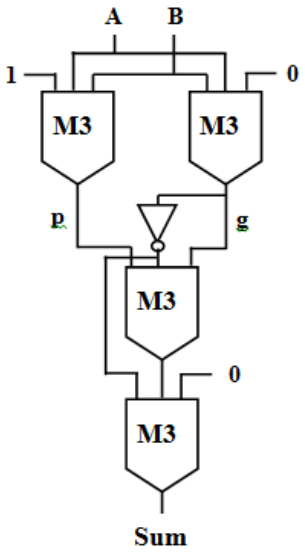


Figure 8. Schematic Diagram of 1-bit Pudi Adder [36]

Where, *g=AB* and *p=A+B*

The schematic of a 1-bit Pudi adder is shown in Figure 8. An n-bit Pudi adder requires $8n-3\log_2(n)-4$, majority gates, *'n'* inverters and $n(\log_2 n-3)+\log_2 n+3n+3$, wire crossovers. The delay of an n-bit Pudi adder is $\frac{2\log_2 n+3}{4}+\frac{n(\log_2 n-2)}{32}$.

Qanbari and Nadooshan Adder

The output carry is computed by a three-input majority gate and then the carry is inverted and is given as input to two inputs of the five-input majority gate [61]. The other three inputs of five-input majority gate are *A, B,* and C_{in} respectively. The output of the five-input majority gate generates the *'Sum'* output. The output *'Sum'* and *'*C_{out}*'* is calculated by equations (11).

$$Sum = M5(A, B, C_{in}, \overline{C}_{out}, \overline{C}_{out}) \tag{11}$$

Bibhash Sen Adder

This multilayer adder employs one five-input majority gate, one three-input majority gate and computes the *'Sum'* output in just two clock zones [47]. The output *'Sum'* is computed by equation (11). The output carry C_{out} is computed according to equation (6) using a three-input majority gate in the first layer and is directly forwarded to the output. It just needs one clock zone. Then, the C_{out} is transmitted upwards by placing a cell in the second layer. This output carry signal is finally fed into the five-input majority gate in the third layer. Inputs *A*, *B*, and C_{in} are applied in the first layer, propagated to third layer by vertically stacked cells and supplied as input to the five-input majority gate. The five-input majority gate generates the output *Sum*.

6. Performance Metrics of QCA Adders

QCA nanotechnology has been emerging as a prospective candidate to replace CMOS technology in future digital circuits. The most of the performance metrics of QCA circuits are mapped from CMOS technology and used to evaluate QCA circuits. Being a new technology, there is a need to investigate the suitable performance metrics for this nanotechnology. W. Liu *et al.* [39] proposed new metrics for QCA circuits and also formulated new cost functions for optimization of QCA circuits. They found that the major metrics are- number of majority/inverter gates, propagation delay, and number and type of wire crossovers. Hence, these performance metrics and cost functions are considered to compare QCA circuits.

Number of majority/inverter gates

A typical QCA circuit comprises of three-input majority gates and inverters. Both of these are main computing gates in QCA technology, any digital circuit can be realized from these. So, the numbers of majority and inverter gates basically affect complexity and area of a QCA circuit. Also, these days five-input majority gates are also used to realize complex digital functions and to reduce the number of levels of three-input majority gates required.

Number and type of wire crossovers

In QCA circuits, wire crossovers play very important role in deciding complexity and area computations of QCA circuits. The crossing of two wires carrying two different signals is a critical issue in QCA nanotechnology. There are two types of wire crossovers in QCA circuits- coplanar crossings and multi-layer wire crossings. In coplanar wire crossing QCA cells are arranged in one layer only and require high precision in alignment. In multi-layer wire crossovers, QCA cells are arranged in multiple-layers. The fabrication cost of this kind of wire crossover is high as compared to coplanar wire crossover as minimum atleast three layers are needed. Also accurate distance between two vertical cells is required for achieving desired kink energy. The equation (12) is generally used to approximate cost of multi-layer crossing [39]:

$$Cost_{ML} = n \times Cost_{CP} \tag{12}$$

Where, $Cost_{CP}$ is the cost of a coplanar wire crossover, $Cost_{ML}$ is the cost of a multi-layer wire crossover and *'n'* is multiplying factor. The value of *'n'* is typically assumed 3 as multi-layer wire crossovers use at least three different layer. The wire crossovers impose implementation constraints in designing complex QCA circuits. The number of wire crossovers should be minimum.

Propagation Delay (Latency)

It is most important index of speed of a QCA circuit. The number of clock zones is measure of propagation delay. A clock zone is $1/4^{th}$ of a clock period. Lesser the number of clock zones required in a QCA circuit, better is the speed. The number of clocking zones used in a QCA circuit is a measure of delay or latency.

A generalized QCA cost function [39] based on the number of majority gates (M) and inverters (I), number and type of wire crossover (C), and the propagation delay (T) as described by equation (13):

$$Cost_{QCA} = (M^k + I + C^l) \times T^p \qquad 1 \leq k, l, p \qquad (13)$$

Table 2. Comparison of n-bit Coplanar QCA Full Adders

Coplanar Adders	Basic Full Adder Structure	Type and No. of Majority Gates used	No. of Inverters	No. of wire-crossovers	Delay (Cycles)	No. of QCA Cells
Tougaw and Lent [5]	Tougaw and Lent	Three-input=5n	3n	9n	n + 1/4	192
Wang [23]	Wang	Three-input =3n	2n	6n	n + 1/4	145
Hanninen and Takala [31]	Wang	Three-input=3n	2n	3n	n+1	102
D. Abedi [55]	Wang	Three-input=3n	2n	Not Required	n	59
S. Hashemi and K. Navi [58]	M. R. Azghadi	Three-input=1n Five Input=1n	2n	Not Required	n + 1/4	71
M. R. Azghadi [60]	M. R. Azghadi	Three-input=1n Five Input=1n	1n	Not Required	n + 1/2	NS*

NS*- Not Specified

Table 3. Comparison of n-bit Multilayer QCA Full Adders

Multi-Layer Adders	Basic Full Adder Structure	Type and No. of Majority Gates used	No. of Inverters	No. of wire-crossovers	Delay (Cycles)	No. of QCA Cells
Zhang [24]	Wang	Three-input=3n	2n	3n	n	108
H. Cho [25]	Wang	Three-input =3n	2n	2n	$\frac{n+2}{4}$	86
Pudi and Sridharan [36]	Pudi and Sridharan	Three- input= $8n-3\log_2(n)-4$	n	$n(\log_2 n-3)+\log_2 n+3n+3$	$\frac{2\log_2 n+3}{4}+\frac{n(\log_2 n-2)}{32}$	94
Qanbari and Nadooshan [61]	M. R. Azghadi	Three-input=1n Five Input=1n	3n	2n	$\frac{3}{4}n$	63
A. N. Bahar and S. Waheed [59]	M. R. Azghadi	Three-input=1n Five Input=1n	2n	0	$\frac{3}{4}n$	48
Bibhash Sen [47]	M. R. Azghadi	Three-input=1n Five Input=1n	0	0	$\frac{1}{2}n$	31

Where, *k, l, p* are the exponential weightings for number of majority gates, wire crossovers count and propagation delay in equation (13) respectively. A QCA circuit can be optimized for different performance metrics according to weightings assigned to k, l, and p.

The Table 2 shows comparison of n-bit coplanar QCA full adders and Table 3 shows comparison of n-bit multilayer QCA full adders reported in literature. The comparison has been carried out in terms of number of majority/inverter gates, type and number of wire-crossovers, propagation delay, and QCA cells used in QCA layout of various adders.

7. Cost Function Computations for QCA Adders

The cost functions values have been calculated for 1-bit coplanar and multilayer QCA full adders using QCA cost function described by equation (13). The coplanar QCA full adder structures considered for cost function computations are Taugaw and Lent, Wang, Hänninen, D. Abedi, S. Hashemi and K. Navi, and M. R. R. Azghadi. The cost function has been computed for multilayer QCA full adder structures like Zhang, H. Cho, Pudi and Sridharan, Qanbari and Nadooshan, Qanbari and Nadooshan, A. N. Bahar and S. Waheed , and B. Sen respectively**.** The cost function has been computed for QCA adder structures by giving higher priority to complexity. As complexity of a QCA circuit is decided by number of majority gates and number and type of wire crossovers, higher priority has been given to k=2 and l=2. The cost of a multilayer wire crossover has been taken three times of a coplanar wire crossover. From computations, we observed that Taugaw and Lent adder is most complex from complexity point of view while D. Abedi adder is least complex. Also S. Hashemi and K. Navi, and M. R. R. Azghadi adder are less complex coplanar adder structures. Similarly, from multilayer adders Pudi and Sridharan adder is most complex while B. Sen adder is least complex. The five-input majority gate is considered equivalent to two three-input majority gates as it has 10 QCA cells and also 5

number of wires are required for it. The Figure 9 and 10 depicts the bar-graph comparison of cost function computations performed for 1-bit coplanar and multilayer QCA adders.

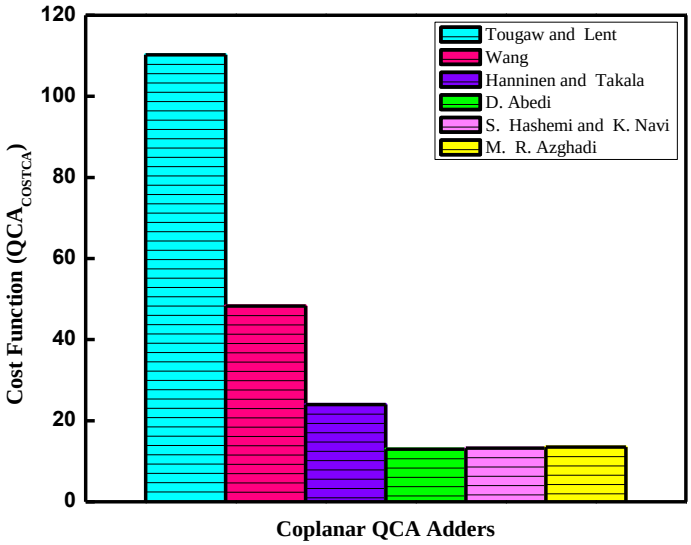


Figure 9. Cost Function for Coplanar QCA Adders

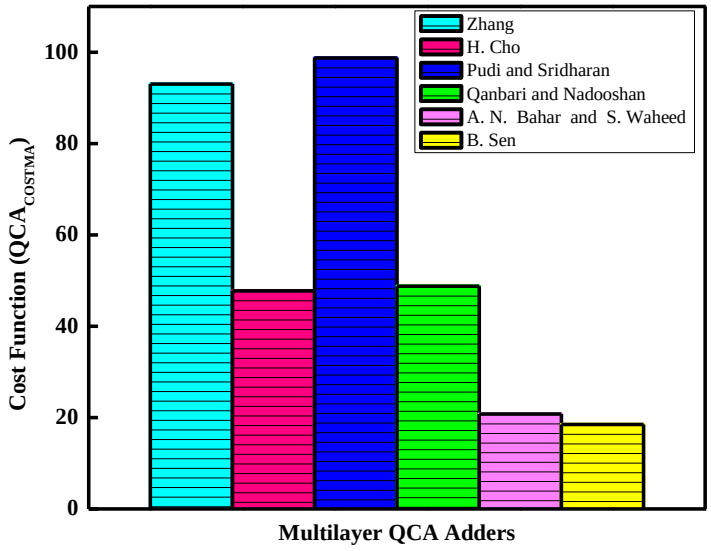


Figure 10. Cost Function for Multilayer QCA Adders

8. Conclusion

The continuous scaling down of feature size has pushed CMOS technology to approach its practical and theoretical limits. Lot of research efforts at nanoscale are in progress to explore alternate viable technologies for future integrated circuits. QCA is emerging as a potential technology that could be used in future computing circuits/systems replacing existing Silicon technology. This paper presents an introduction to QCA technology, QCA fundamentals, QCA technology developments, evolution of QCA adders, QCA full adder designs, performance metrics, and cost function computations for coplanar and multilayer QCA 1-bit full adders. The QCA adder designs have been compared in terms of adder type (coplanar or multilayer), basic full adder structure type, type and number of majority gates used, number of inverters, number of wire-crossovers, delay, and number

of QCA cells. Also, the cost functions have been computed for both coplanar and multilayer QCA adders by giving higher priority to complexity.

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