# **Design PD Functional Based FPGA Controller for FOD Systems**

Mohammad Hadi Mazloom<sup>1,2</sup>, Farzin Piltan<sup>1</sup>, Amirzubir Sahamijoo<sup>1</sup>, Hootan Ghiasi<sup>1</sup>, Mohammad Reza Avazpour<sup>1</sup> and Nasri B. Sulaiman<sup>1,3</sup>

<sup>1</sup>Intelligent Systems and Robotics Lab, Iranian Institute of Advanced Science and Technology (IRAN SSP), Shiraz/Iran
<sup>2</sup>School of Electrical, Computer and Energy Engineering, College of Engineering, Arizona State University (ASU), USA
<sup>3</sup>Department of Electrical and Electronic Engineering, Faculty of Engineering, University Putra Malaysia, Malaysia
piltan\_f@iranssp.org, WWW.IRANSSP.ORG/English

#### Abstract

Robust controller design for nonlinear systems with unknown dynamics (delay system) the impact of intense activity between connections can be considered as a challenge in this research. In order to reduce delays in the system resistant and the non-linear technique called variable structure control method is used. Variable structure control method is a type of non-linear controllers, although variable structure control technique, control is stable, with high reliability in environments that respond favorably almost unknown but has substantial limitations fluctuations (vibrations) high-frequency is. To fix this problem, saturated nonlinear function method was used.

Many nonlinear controllers need to chip control with low volume, functionality, accuracy, and speed are high. Programmable integrated circuits are capable of solving these challenges. Programmable integrated circuits to design nonlinear variable structure controller optimized linear controller on a single chip is used. Having designed to speed up the response of the SPARTAN-3E in Xilinx programmable integrated circuit used. This technique is designed to control the programmable integrated circuit SPARTAN-3E, computational speed controller is 30.2 ns and a maximum frequency of 63.7 MHZ circuit.

*Keywords*: real-time operation, Field Programmable Gate Array (FPGA), Variable Structure Control algorithm, first order delay (FOD) system, VHDL, Xilinx

#### 1. First Order Delay (FOD) System

System or plant is a set of components which work together to follow a certain objective. In this research, first order delay is system. First order delay (FOD) system is a type of nonlinear and time variant system. A first order model can represent many industrial processes; equation (1) shows the mathematical plant model (in *s-plane*). Discrete transfer function of this model has obtained using ZOH method, and the selected sampling period (T) is 0.1, equation (2) shows the discrete transfer functions, (in *z-plane*)[1-5].

$$CS_1(s) = \frac{1}{S+1} \tag{1}$$

and;

$$CS_1(z) = \frac{0.09516}{Z - 0.9048}$$
,  $T = 0.1$  (2)

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The time delay occurs when a sensor or an actuator are used with a physical separation. Equation (3) shows the mathematical plant model (in *s-plane*). Discrete transfer functions of this model has been obtained using ZOH method, and the selected sampling period (T) is 0.1, equation (4 and 5) show the discrete transfer functions, (in *z-plane*).

$$CS_2(s) = \frac{1}{S^2 \times (S+1)} \tag{3}$$

$$CS_2(z) = Z^{-2} \times CS_1(z) \tag{4}$$

$$CS_2(z) = Z^{-2} \times \frac{0.09516}{Z - 0.9048}, T = 0.1$$
 (5)

#### 2. Control Technique

Digital nonlinear controller design and its implementation on the FPGA to optimize and reduce delays, is the main challenge in this research. According to the technology boom of the main concerns of manufacturers, system design is similar to human performance. Until a few years ago, one of the most important limitations in control systems design, speed, and volume of data transfer in real systems. This was due to nonlinear control systems design constraints, resulting in decreased accuracy and limitations of the system is used. Due to the very high flexibility, speed and high design, FPGAs are the main tools for control system design for nonlinear control systems. Hence, the need to use powerful integrated circuits, FPGA is clearly identified in this study.

The challenge of selecting appropriate control techniques to improve system response delay arises. Control strategy in these systems can be divided into two general groups:

• Linear Control Method

• Non-linear control method

The linear controller output-input relationship is just a first order function. The controllers have no dependence on system dynamics model.

Non-linear controllers are divided into two main groups:

• model-reference nonlinear control systems: the function of the controller is generally based on nonlinear dynamics and behavior of the system.

• Model-free nonlinear controller: This technique is based on a simulation of the system.

These techniques are divided into two groups:

- Function-based nonlinear control techniques
- Smart nonlinear control

Linear controller design of nonlinear controller is much easier, but due to the use of non-linear control techniques in this research mean?

For optimal linear controllers in the system draws the following factors:

More linear response reduction methods (limiting) velocity and acceleration, it would be because of limitations in the design and system's operation is incompatible with the development of technology. Therefore, in this study alone are not applied linear controller. According to controller problems linear, nonlinear control method with variable function used in this study. In this control method to solve the problem of delay initially defined a fixed or variable level. If the correct determination of the level, speed and quality are much improved system response.

Based on the research of control systems can be designed in two environments:

• Control systems design supports computer-aided design: In this method, the system processing unit is implemented on a computer system. In this way computer systems in the system that should be discussed as the most important challenge is commutative system.

• Control systems design and programmable micro-controller on the system, in this way the movement is easily solved because the micro-controller on a single chip is designed. In the following discussion of the volume and speed of information processing comes to powerful control systems are programmable as proposed a solution.

According to above the main four objectives to design controllers are: stability, robust, minimum error and reliability. Linear PID controller is model-free controller and this controller is not reliable. One of the robust nonlinear controllers which have been analyzed by many researchers especially in recent years to control of nonlinear systems is sliding mode controller (SMC). Sliding mode controller (SMC) is robust conventional nonlinear controller in a partly uncertain dynamic system's parameters. This conventional nonlinear controller is used in several applications such as in robotics, process control, aerospace and power electronics. This controller can solve two most important challenging topics in control theory, stability and robustness [6-7]. The main idea to design sliding mode control is based on the following formulation;

$$\boldsymbol{\tau}_{(\boldsymbol{q},t)} = \begin{cases} \boldsymbol{\tau}_{i}^{+}(\boldsymbol{q},t) & \text{if } S_{i} > 0\\ \boldsymbol{\tau}_{i}^{-}(\boldsymbol{q},t) & \text{if } S_{i} < 0 \end{cases}$$
(6)

where  $S_i$  is sliding surface (switching surface), i = 1, 2, ..., n for *MIMO* system,  $\tau_i(q, t)$  is the  $i^{th}$  torque. According to above formulation the main part of this control theory is switching part this idea is caused to increase the speed of response. Sliding mode controller is divided into two main sub parts:

- Discontinues controller( $\tau_{dis}$ )
- Equivalent controller( $\tau_{eq}$ )

Discontinues controller is used to design suitable tracking performance based on very fast switching. This part of controller is work based on the linear type methodology; therefore it can be PD, PI and PID. Fast switching or discontinuous part have essential role to achieve to good trajectory following, but it is caused system instability and chattering phenomenon. Chattering phenomenon is one of the main challenges in conventional sliding mode controller and it can causes some important mechanical problems such as saturation and heats the mechanical parts of FODS or drivers.

To reduce or eliminate the chattering, two main methods are used as follows:

- boundary layer saturation method
- artificial intelligence based method

The dynamic formulation of nonlinear single input system is defined by:

$$x^{(n)} = f(\vec{x}) + b(\vec{x})u \tag{7}$$

**u** is the vector of control input,  $x^{(n)}$  is the  $n^{th}$  derivation of x,  $x = [x, \dot{x}, \ddot{x}, ..., x^{(n-1)}]^T$  is the state vector, f(x) is unknown or uncertainty, and b(x) is known *switching (SIGN)* function. The main target to design sliding mode controller is high speed train and high tracking accuracy to the desired joint variables;  $x_d = [x_d, \dot{x}_d, \ddot{x}_d, ..., x_d^{(n-1)}]^T$ , according to actual and desired joint variables, the trucking error vector is defined by:

$$\widetilde{\mathbf{x}} = \mathbf{x}_d - \mathbf{x}_a = [\widetilde{\mathbf{x}}, \dots, \widetilde{\mathbf{x}}^{(n-1)}]^T$$
(8)

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According to the sliding mode controller theory, the main important part to design this controller is sliding surface, a time-varying sliding surface s(x, t) in the state space  $\mathbb{R}^n$  is given by the following formulation:

$$s(x,t) = \left(\frac{d}{dt} + \lambda\right)^{n-1} \widetilde{x} = 0 \tag{9}$$

 $\lambda$  is the sliding surface slope coefficient and it is positive constant. The sliding surface can be defined as Proportional-Derivative (PD), Proportional-Integral (PI) and the Proportional-Integral-Derivative (PID). The following formulations represented the three groups are:

$$S_{PD} = \lambda e + \dot{e} \tag{10}$$

$$s(x,t) = \left(\frac{d}{dt} + \lambda\right)^{n-1} \left(\int_0^t \widetilde{x} \, dt\right) = \mathbf{0}$$
<sup>(11)</sup>

$$S_{PI} = \lambda e + (\frac{\lambda}{2})^2 \sum e$$
<sup>(12)</sup>

$$S_{PID} = \lambda e + \dot{e} + (\frac{\lambda}{2})^2 \sum e$$
(13)

Integral part of sliding surface is used to decrease the steady state error in sliding mode controller. To have the stability and minimum error in sliding mode controller, the main objective is kept the sliding surface slope s(x, t) near to the zero. Therefore, one of the common strategies is to find input U outside of s(x, t).

$$\frac{1}{2}\frac{d}{dt}s^2(x,t) \le -\zeta |s(x,t)| \tag{14}$$

 $\zeta$  is positive constant.

If 
$$S(0) > 0 \rightarrow \dot{S}(t) \le -\zeta$$
 (15)

Derivative term of (s) is eliminated by limited integral from t=0 to t= $t_{reach}$ 

$$\int_{t=0}^{t=t_{reach}} \dot{S}(t) \leq -\int_{t=0}^{t=t_{reach}} \eta \to S(t_{reach}) - S(0) \leq -\zeta(t_{reach} - 0)$$
(16)

 $t_{reach}$  is the time that trajectories reach to the sliding surface. If  $S_{t_{reach}} = 0$  the formulation of  $t_{reach}$  calculated by;

$$0 - S(0) \le -\eta(t_{reach}) \to t_{reach} \le \frac{S(0)}{\zeta}$$
If  $S(0) < 0$ 
(17)

$$0 - S(\mathbf{0}) \le -\eta(t_{reach}) \to S(\mathbf{0}) \le -\zeta(t_{reach}) \to t_{reach} \le \frac{|S(\mathbf{0})|}{\eta}$$
(18)

Above formulation guarantees time to reach the sliding surface is smaller than  $\frac{|S(0)|}{z}$  since the trajectories are outside of S(t).

$$if S_{t_{reach}} = S(\mathbf{0}) \to error(x - x_d) = \mathbf{0}$$
(19)

According to above discussion the formulation of sliding surface (S) is defined as

$$s(x,t) = \left(\frac{d}{dt} + \lambda\right) \quad \tilde{x} = (\dot{x} - \dot{x}_d) + \lambda(x - x_d) \tag{20}$$

The change of sliding surface  $(\dot{S})$  is;

$$\dot{\mathbf{S}} = (\ddot{\mathbf{x}} - \ddot{\mathbf{x}}_{d}) + \lambda(\dot{\mathbf{x}} - \dot{\mathbf{x}}_{d}) \tag{21}$$

According to the formulation of the second order system, a simple solution to get the sliding condition when the dynamic parameters have uncertainty in parameters or external disturbance is the switching control law:

$$U_{dis} = K(\vec{x}, t) \cdot \text{sgn}(s) \tag{22}$$

The switching function **sgn**(*s*) is defined as

$$sgn(s) = \begin{cases} 1 & s > 0 \\ -1 & s < 0 \\ 0 & s = 0 \end{cases}$$
(23)

The  $K(\vec{x}, t)$  is the positive constant and the sliding surface can be PD, PI and PID. In PD sliding surface, the change of sliding surface calculated as;

$$S_{PD} = \lambda e + \dot{e} \to \dot{S}_{PD} = \lambda \dot{e} + \ddot{e}$$
(24)

The discontinuous switching term  $(U_{dis})$  is computed as;

$$U_{dis} = K \cdot \operatorname{sgn}(S) \tag{25}$$

$$U_{dis-PD} = K \cdot \operatorname{sgn}(\lambda e + \dot{e}) \tag{26}$$

$$U_{dis-PI} = K \cdot \text{sgn}\left(\lambda e + \left(\frac{\lambda}{2}\right)^2 \sum e\right)$$
<sup>(27)</sup>

The discontinuous switching part is;

$$U_{dis-PID} = K \cdot \operatorname{sgn}\left(\lambda e + \dot{e} + \left(\frac{\lambda}{2}\right)^2 \sum e\right)$$
(28)

Figure 1 shows the trajectory following in SIGN functional base controller. According to this Figure, system's delay time is about 5 seconds. Sliding mode controller reduces the delay time from 5 seconds to about 0.9 seconds. However, SMC reduce the performance delay time but high frequency oscillation is the main challenge in this design.

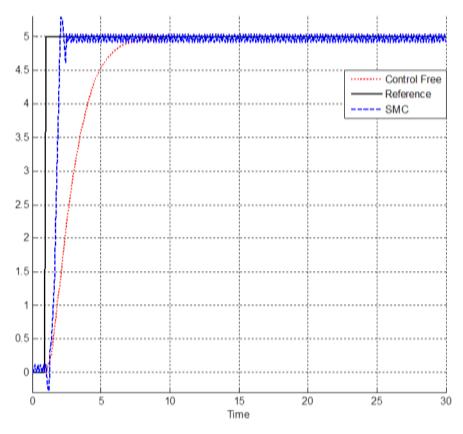


Figure 1. Trajectory Following Reference Signal, Control Free, SMC

To test the power of disturbance rejection, sliding mode controller is used as follows. Figure 2 shows the power of disturbance rejection in SMC. Regarding to Figure 2, SMC is a robust controller but it has the high frequency oscillation challenge in certain and uncertain condition.

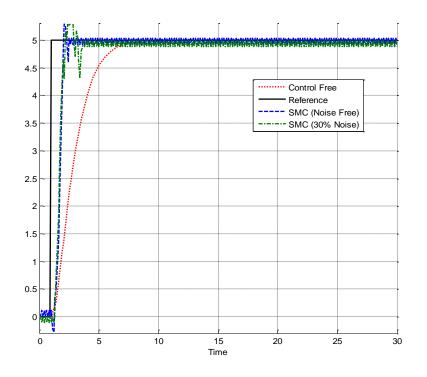


Figure 2. Power of Disturbance Rejection Reference Signal, Control Free, SMC

To design FPGA-based SMC following steps are introduced [9]:

- design Derivative algorithm
- design sliding surface slope (S) algorithm

The following formulation shows the derivative algorithm:

$$d(e) = \frac{Din(t) - Din(t-1)}{\Delta t} = (Din(k+1) - Din(k)) \times sample time$$

$$Din = q_d - q_a$$
(30)

However  $q_d$  and  $q_a$  are 30 bits but Din is 40 bits. In derivative algorithm, delay time is the main challenge. In this research the value of sample time is "01010". To design FPGA-based sliding surface slope algorithm the following formulation is used.

$$U_{S} = \lambda \times e + \left(\frac{de}{dt}\right) = \lambda \times e + \dot{e}$$
<sup>(31)</sup>

The device utilization summary shows in Figure 3.

Device Utilization Summary (estimated values)				
Logic Utilization	Used	Available	Utilization	
Number of Slices	178	14752	1%	
Number of Slice Flip Flops	73	29504	0%	
Number of 4 input LUTs	253	29504	0%	
Number of bonded IOBs	98	304	32%	
Number of MULT18X18SIOs	9	36	25%	
Number of GCLKs	2	24	8%	

**Figure 3. Device Utilization Summary** 

Figure 4 shows the HDL synthesis report in traditional SMC.

HDL Synthesis Report		
Macro Statistics		
# Multipliers	:	3
40x5-bit multiplier	:	1
40x6-bit multiplier	:	2
# Adders/Subtractors	:	3
40-bit adder	:	1
40-bit subtractor	:	2
# Registers	:	5
1-bit register	:	1
40-bit register	:	4
# Comparators	:	2
40-bit comparator greater	:	1
40-bit comparator less	:	1
# Multiplexers	:	1
40-bit 4-to-1 multiplexer	:	1

#### Figure 4. HDL Synthesis Report: SMC Algorithm

Timing summary has played an important role in FPGA-based control design. Figure 5 shows the timing summary in traditional SMC.

```
Timing Summary:
______
Speed Grade: -4
Minimum period: 15.716ns (Maximum Frequency: 63.629MHz)
Minimum input arrival time before clock: 4.407ns
Maximum output required time after clock: 30.286ns
Maximum combinational path delay: No path found
Timing Detail:
______
All values displayed in nanoseconds (ns)
```

## Figure 5. Timing Summary: SMC Algorithm

Regarding to Figure 5, the Maximum frequency in this design is 63.629 MHz but the maximum frequency for input in this design is about 23 MHz. However the maximum frequency in this design is about 63.6 MHz but the maximum output frequency is about 27.1 MHz. The rate of error in SMC shows in Figure 6. According to this Figure the error in t=133 nano seconds is about 5.1, it means SMC has undershoot.

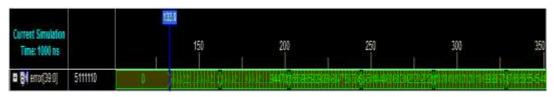


Figure 6. Error in SMC at t=133 ns

Figure 7 shows the error rate at t=200 ns for SMC.

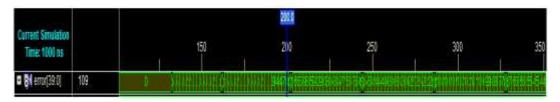


Figure 7. Error in SMC at t=200 ns

According to Figure 7 the rate of error from 5.1 at 133 ns change to 0.000109 at t=200 ns. According to this Figure, it has high frequency oscillation in this technique.

To attenuate the chattering challenge, linear boundary layer method based on saturation function is introduced. In this method, we introduced saturation function in the sliding mode control law instead of the switching (sign) function. The saturation (linear) method with small neighborhood of the switching surface is calculated as:

$$\boldsymbol{B}(\boldsymbol{t}) = \{\boldsymbol{x}, |\boldsymbol{S}(\boldsymbol{t})| \le \emptyset\}; \emptyset > 0 \tag{32}$$

where  $\emptyset$  is the boundary layer thickness. Consequently, the sliding mode function can be written by;

$$U = K(\vec{x}, t) \cdot \operatorname{Sat}\left(\frac{S}{\emptyset}\right)$$
(33)

While saturation function formulation ( $\operatorname{Sat}(S_{\emptyset})$ ) is as follows

$$\operatorname{sat}\left(\frac{s}{\phi}\right) = \begin{cases} 1 & \left(\frac{s}{\phi} > 1\right) \\ -1 & \left(\frac{s}{\phi} < -1\right) \\ \frac{s}{\phi} & \left(-1 < \frac{s}{\phi} < 1\right) \end{cases}$$
(34)

Considering the above points, to reduce chattering phenomenon in sliding mode controller based on saturation function, the following formulation is used:

$$U_{sat} = K \cdot \operatorname{sat}\left(\frac{S}{\phi}\right) \tag{35}$$

Figure 8 shows the trajectory following in boundary layer SMC. According to the following Figure, this method eliminate the high frequency oscillation as well as improve the trajectory following. The main challenge in this method is time response.

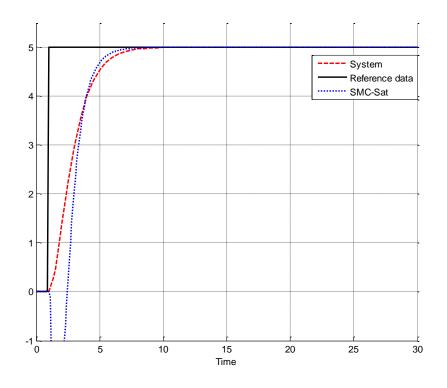


Figure 8. Trajectory Following Reference Signal, Control Free, SMC-Sat

To test the power of disturbance rejection, the band limited white noise apply to boundary layer sliding mode controller. Figure 9 shows the power of disturbance rejection in boundary layer sliding mode controller.

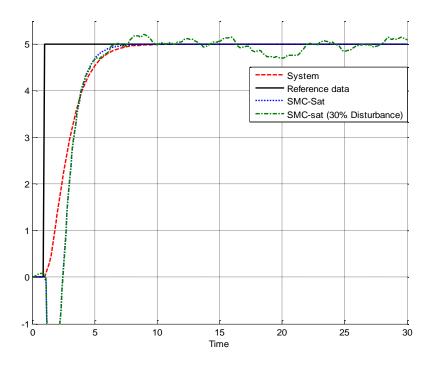


Figure 9. Disturbance Rejection Reference Signal, Control Free, SMC-Sat

According to above Figure this method has a challenge in stability and robustness. After design FPGA based boundary layer SMC the timing report in this design is as Figure 10:

```
Timing Summary:
______
Speed Grade: -4
Minimum period: 15.716ns (Maximum Frequency: 63.629MHz)
Minimum input arrival time before clock: 4.362ns
Maximum output required time after clock: 36.790ns
Maximum combinational path delay: No path found
Timing Detail:
______
All values displayed in nanoseconds (ns)
```

#### Figure 10. Timing Summary: SMC Algorithm

However the input frequency is about 63.6 MHz but the maximum output required frequency is about 33.1 MHz, it means that the output systems frequency is about 51% of input signal. Figure 11 shows the error report in this algorithm. According to this Figure the rate of error at t=132 ns is about -0.000112.



Figure 11. Error in Boundary Layer SMC at t=132 ns

Figure 12 shows the rate of error at t=140 ns. In this time, the error is about zero.

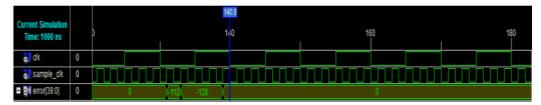


Figure 12. Error in Boundary Layer SMC at t=140 ns

### 3. Conclusion

In this research, PD FPGA-based algorithm for first order delay system is design and analysis. From the design and simulation results, it can be concluded that; higher execution speed versus small chip size is achieved by design FPGA-based PD controller with the simplified structure. In output required frequency point of view, the maximum output required frequency in traditional SMC is about 33.1 MHz and the maximum output frequency in boundary layer SMC is about 27.1 MHz. In error point of view, the rate of error in traditional SMC at t=132 ns is about 5.1 and in boundary layer SMC is about -0.000112.

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#### Project Title:" Design a Micro-electronic Based Nonlinear Controller for First Order Delay System"

Iranian center of Advance Science and Technology (IRAN SSP) is one of the independent research centers specializing in research and training across of Control and Automation, Electrical and Electronic Engineering, and Mechatronics & Robotics in Iran. At IRAN SSP research center, we are united and energized by one mission to discover and develop innovative engineering methodology that solve the most important challenges in field of advance science and technology. The IRAN SSP Center is instead to fill a long standing void in applied engineering by linking the training a development function one side and policy research on the other. This center divided into two main units:

- Education unit
- Research and Development unit

### References

- [1] K. Gu, "An integral inequality in the stability problem of time-delay systems", Decision and Control, 2000. Proceedings of the 39th IEEE Conference on. IEEE, vol. 3, (2000).
- [2] W. Michiels and S.-I. Niculescu, "Stability, Control and Computation for Time-delay Systems: An Eigenvalue-based Approach", Siam, vol. 27, (2014).
- [3] L. Wu, X. Su and P. Shi, "Sliding mode control with bounded *L*2 gain performance of Markovian jump singular time-delay systems", Automatica, vol. 48, no. 8, (**2012**), pp. 1929-1933.
- [4] V. Goyal, V. K. Deolia and T. Nath Sharma, "Neural Network Based Sliding Mode Control for Uncertain Discrete-Time Nonlinear Systems with Time-Varying Delay", International Journal of Computational Intelligence Research, vol. 12, no. 2, (2016), pp. 125-138.
- [5] S. Xu, "New insight into delay-dependent stability of time-delay systems", International Journal of Robust and Nonlinear Control, vol. 25, no. 7, (2015), pp. 961-970.
- [6] S. Namvarrechi, S. Soltani, I. Nazari, A. Roshanzamir and A. Jahed, "Design Single Chip Micro-Based Controller for First Order Delays System", International Journal of Hybrid Information Technology, vol. 9, no. 5, (2016), pp. 71-98.
- [7] M. Abdelati, "FPGA-Based PID Controller Implementation", IUG Journal of Natural Studies, vol. 14, no. 1, (2016).
- [8] R. A. Juan-Manuel, T. A. Saul, V. S. Jose-Emilio and A. F. Marco-Antonio, "FPGA EMBEDDED PD CONTROL OF A 1 DOF MANIPULATOR WITH A PNEUMATIC ACTUATOR." International Journal of Robotics and Automation, vol. 31, no. 3, (2016).
- [9] G. Himunzowa and F. Smith, "FPGA Based Self-tuning PI Controller Using IFT Technique", In Automation Control Theory Perspectives in Intelligent Systems, Springer International Publishing, (2016), pp. 203-216.

## Authors



**Mohammad Hadi Mazloom**, he is currently research assistant at Institute of Advanced Science and Technology, Research Center, IRAN SSP. He is research assistant of team (8 researchers) to design a Micro-electronic Based nonlinear controller for first order delay system since Jan, 2015 to now, research student (21 researchers) to design high precision and fast dynamic controller for multi-degrees of freedom actuator since 2014 to date, and published 3 journal papers since 2014 to date. His current research interests are nonlinear control, artificial control system, Microelectronic Device, and HDL design.



Farzin Piltan, he is an outstanding scientist in the field of Electronics and Control engineering with expertise in the areas of nonlinear systems, robotics, and microelectronic control. Mr. Piltan is an advanced degree holder in his field. Currently, Mr. Piltan is the Head of Mechatronics, Intelligent System, and Robotics Laboratory at the Iranian Institute of Advanced Science and Technology (IRAN SSP). Mr. Piltan led several high impact projects involving more than 150 researchers from countries around the world including Iran, Finland, Italy, Germany, South Korea, Australia, and the United States. Mr. Piltan has authored or co-authored more than 140 papers in academic journals, conference papers and book chapters. His papers have been cited at least 3900 times by independent and dependent researchers from around the world including Iran, Algeria, Pakistan, India, China, Malaysia, Egypt, Columbia, Canada, United Kingdom, Turkey, Taiwan, Japan, South Korea, Italy, France, Thailand, Brazil and more. Moreover, Mr. Piltan has peer-reviewed at least 23 manuscripts for respected international journals in his field. Mr. Piltan will also serve as a technical committee member of the upcoming EECSI 2015 Conference in Indonesia. Mr. Piltan has served as an editorial board member or journal reviewer of several international journals in his field as follows: International Journal Of Control And Automation (IJCA). Australia, ISSN: 2005-4297. International Journal of Intelligent System and Applications (IJISA), Hong Kong, ISSN: 2074-9058, IAES International Journal Of Robotics And Automation, Malaysia, ISSN:2089-4856, International Journal of Reconfigurable and Embedded Systems, Malaysia, ISSN:2089-4864.

Mr. Piltan has acquired a formidable repertoire of knowledge and skills and established himself as one of the leading young scientists in his field. Specifically, he has accrued expertise in the design and implementation of intelligent controls in nonlinear systems. Mr. Piltan has employed his remarkable expertise in these areas to make outstanding contributions as detailed follows:Nonlinear control for industrial robot manipulator (2010-IRAN SSP), Intelligent Tuning The Rate Of Fuel Ratio In Internal Combustion Engine (2011-IRANSSP), Design High Precision and Fast Dynamic Controller For Multi-Degrees Of Freedom Actuator (2013-IRANSSP), Research on Full Digital Control for Nonlinear Systems (2011-IRANSSP), Micro-Electronic Based Intelligent Nonlinear Controller (2015-IRANSSP), Design a Micro-Electronic Based Nonlinear Controller for First Order Delay System (2015-IRANSSP).

The above original accomplishments clearly demonstrate that Mr. Piltan has performed original research and that he has gained a distinguished reputation as an outstanding scientist in the field of electronics and control engineering. Mr. Piltan has a tremendous and unique set of skills, knowledge and background for his current and future work. He possesses a rare combination of academic knowledge and practical skills that are highly valuable for his work. In 2011, he published 28 first author papers, which constitute about 30% of

papers published by the Department of Electrical and Electronic Engineering at University Putra Malaysia. Additionally, his 28 papers represent about 6.25% and 4.13% of all control and system papers published in Malaysia and Iran, respectively, in 2011.



Amirzubir Sahamijoo, he currently is senior research assistant at Institute of Advanced Science and Technology, Research Center, IRAN SSP. He is senior research assistant of team to Design Intelligent FPGA-Based Control Unit to Control of 4-DOF Medical Robot Manipulator since July, 2015 to now, research assistant of team (8 researchers) to design a Micro-electronic Based nonlinear controller for first order delay system since March, 2015 to now, research student (21 researchers) to design high precision and fast dynamic controller for multi-degrees of freedom actuator since 2014 to date, research student (9 researchers) to design Prevent the Risk of Lung Cancer Progression Based on Fuel Ratio Optimization since 2014 to date, and published 4 journal papers since 2014 to date. His current research interests are nonlinear control, artificial control system, Microelectronic Device, Internal Combustion Engine, and HDL design.



**Hootan Ghiasi**, he is currently research assistant at Institute of Advanced Science and Technology, Research Center, IRAN SSP. He is research assistant of team (8 researchers) to design a Microelectronic Based nonlinear controller for first order delay system since Jan, 2015 to now, research student (21 researchers) to design high precision and fast dynamic controller for multi-degrees of freedom actuator since 2014 to date, and published 3 journal papers since 2014 to date. His current research interests are nonlinear control, artificial control system, Microelectronic Device, and HDL Design.



**Mohammad Reza Avazpour**, he is currently research assistant at Institute of Advanced Science and Technology, Research Center, IRAN SSP. He is research assistant of team (8 researchers) to design a Micro-electronic Based nonlinear controller for first order delay system since Jan, 2015 to now, research student (21 researchers) to design high precision and fast dynamic controller for multi-degrees of freedom actuator since 2014 to date, and published 3 journal papers since 2014 to date. His current research interests are nonlinear control, artificial control system, Microelectronic Device, and HDL design.



**Nasri Sulaiman**, he is a Senior Lecturer in the Department Electrical and Electronic Engineering at the Universiti Purta Malaysia (UPM), which is one of the leading research universities in Malaysia. He is a supervisor and senior researcher at research and training center called, Iranian Institute of Advanced Science and technology (Iranssp) since 2012. He obtained his M.Sc. from the University of Southampton (UK), and Ph.D. in Microelectronics from the University of Edinburgh (UK). He has published more than 80 technical papers related to control and system engineering, including several co-authored papers with Mr. Piltan. He has been invited to

present his research at numerous national and international conferences. He has supervised many graduate students at doctoral and masters level. He is an outstanding scientist in the field of Micro-Electronics.

Dr. Nasri Sulaiman advisor and supervisor of several high impact projects involving more than 150 researchers from countries around the world including Iran, Malaysia, Finland, Italy, Germany, South Korea, Australia, and the United States. Dr. Nasri Sulaiman has authored or co-authored more than 80 papers in academic journals, conference papers and book chapters. His papers have been cited at least 3000 times by independent and dependent researchers from around the world including Iran, Algeria, Pakistan, India, China, Malaysia, Egypt, Columbia, Canada, United Kingdom, Turkey, Taiwan, Japan, South Korea, Italy, France, Thailand, Brazil and more.

Dr. Nasri Sulaiman has employed his remarkable expertise in these areas to make outstanding contributions as detailed below:

•Design of a reconfigurable Fast Fourier Transform (FFT) Processor using multi-objective Genetic Algorithms (2008-UPM)

•Power consumption investigation in reconfigurable Fast Fourier Transform (FFT) processor (2010-UPM)

•Crest factor reduction And digital predistortion Implementation in Orthogonal frequency Division multiplexing (ofdm) systems (2011-UPM)

•High Performance Hardware Implementation of a Multi-Objective Genetic Algorithm, (RUGS), Grant amount RM42,000.00, September (2012-UPM)

•Nonlinear control for industrial robot manipulator (2010-IRAN SSP)

•Intelligent Tuning The Rate Of Fuel Ratio In Internal Combustion Engine (2011-IRANSSP)

•Design High Precision and Fast Dynamic Controller For Multi-Degrees Of Freedom Actuator (2013-IRANSSP)

•Research on Full Digital Control for Nonlinear Systems (2011-IRANSSP)

•Micro-Electronic Based Intelligent Nonlinear Controller (2015-IRANSSP)

•Active Robot Controller for Dental Automation (2015-IRANSSP)

•Design a Micro-Electronic Based Nonlinear Controller for First Order Delay System (2015-IRANSSP) International Journal of Hybrid Information Technology Vol. 10, No.1 (2017)