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# SSTL Based Energy Efficient ISCAS'99 Benchmark Circuit Design on FPGA

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***Abstract***

*In this work, we are using frequency scaling as power optimization technique. In frequency scaling, frequency is scaled from 1MHz to 1THz, where intermediate values are 10MHz, 100 MHz, 1 GHz, 10 GHz and 100 GHz. In this paper we have measured the different power dissipation for different SSTL Logic families with the help of frequency scaling. If we are measuring the clock power, logic power and signals power for different logic families at one frequency then these powers comes out to be the same that concludes that these three powers are same for all the SSTL Logic families for some same frequency .But it had been observed that total power (including clocks, logic, signals, IOs, leakage powers) keeps on changing for different SSTL logic families even at one same frequency. If we are operating on frequency of 1MHz, there will be maximum power dissipation in case of SSTL2_II_DCI and minimum power dissipation in case of SSTL15. Similarly if we are operating on frequency of 10MHz, there will be maximum power dissipation again in case of SSTL2_II_DCI and minimum power dissipation in case of SSTL15. Similarly if we are operating on frequency of 100MHz, 1GHz, 10GHz, 100GHz and there will be maximum power dissipation again in case of SSTL2_II_DCI and minimum power dissipation in case of SSTL15 always. But in case of 1THZ frequency the maximum power dissipation is in case of SSTL2_II logic family and minimum power dissipation in case of SSTL18_I_DCI.*

***Keywords:*** *SSTL, Frequency Scaling, FPGA, VLSI, Device Operating Frequency*

## 1. Introduction

A logic family of an integrated circuit is a group of electronic logic gates constructed with compatible logic levels and power supply characteristics within a family. In this paper an approach is made to design the voltage based efficient fire sensor and for that reason we have used four different kinds of Stub Series Terminated Logic (SSTL) IO standards. Voltage based efficient fire sensor have been made by using four different kinds of Stub Series Terminated Logic (SSTL) IO standards [1]. In this paper two standards are being used as a general purpose memory buses which we are (SSTL2) and (SSTL18) [2]. We have also some of the standard that are designed for some specific purpose. JEDEC standard JESD8-15 defines the SSTL18 family and JESD8-9B defines the SSTL2[2]. We have two classes of SSTL2 standards, out of which Class I is being used for unidirectional standards for which a series resistor either of 25 Ω at 2.5V or 20 Ω at 1.8V) needs to be connected to the output of the transmitter [2]. Class II is being used for bidirectional signaling for which we need to connect a resistor of 25 Ω in series to the transceivers's output. [2].Virtex-6 FPGA is capable of supporting both the standards of signaling either it may be single-ended or differential signaling.[2].FSM is widely used in contemporary logic design [3]. ISCAS'99 benchmark circuit is used to test design on

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FPGA [4]. Here, we are using ISCAS'99 benchmark circuit on FPGA in order to make it more energy efficient design. SSTL is already in use in energy efficient design of Parallel Integrator [7], Fire Sensor [8] and Image ALU [9]. Here, we are filling the research gap in design of energy efficient benchmark circuits.

## 2. Results

- ***Power Dissipation With IO Standards at 1 GHz Frequency***

**Table 1. Clock Power, Logic Power, and Signals Power**

| NAME OF THE FAMILY | CLOCKS POWER | LOGIC POWER | SIGNALS POWER |
|---|---|---|---|
| LVCMOS25 | 0.014 | 0.000 | 0.000 |
| SSTL2_I | 0.014 | 0.000 | 0.000 |
| SSTL18_I | 0.014 | 0.000 | 0.000 |
| SSTL2_I_DCI | 0.014 | 0.000 | 0.000 |
| SSTL18_I_DCI | 0.014 | 0.000 | 0.000 |
| SSTL2_II | 0.014 | 0.000 | 0.000 |
| SSTL15 | 0.014 | 0.000 | 0.000 |
| SSTL2_II_DCI | 0.014 | 0.000 | 0.000 |
| SSTL18_II_DCI | 0.014 | 0.000 | 0.000 |
| SSTL15_DCI | 0.014 | 0.000 | 0.000 |

It has been observed that there is no change in clock, logic and signals power in different SSTL logic families at one same frequency (say 1GHZ) at Virtex-6 as shown in Table 1 and Figure 1.

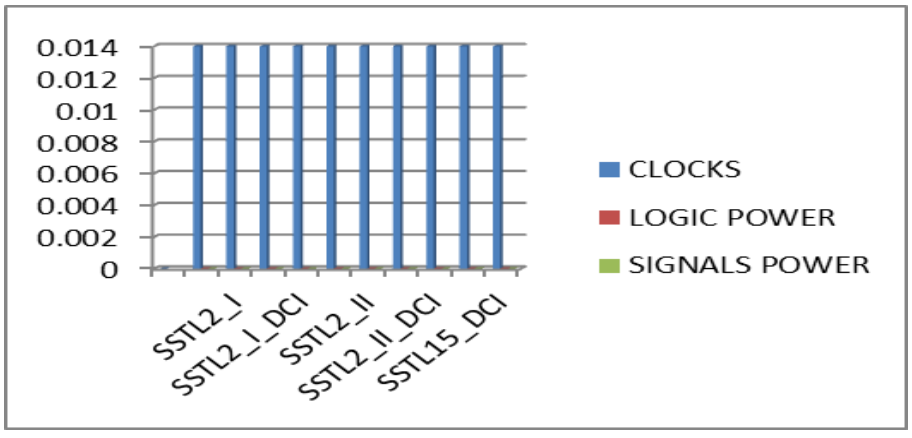


**Figure 1. Dynamic Power Dissipation for Different Logic Families**

- ***Power Dissipation With SSTL Logic at 1 MHz Frequency***

**Table 2. Total Power Dissipation of ISCAS'99 Benchmark Circuits**

| LOGIC FAMILIES | TOTAL POWER DISSIPATION |
|---|---|
| SSTL2_I | 0.786 |
| SSTL18_I | 0.782 |
| SSTL2_I_DCI | 0.916 |
| SSTL18_I_DCI | 0.849 |
| SSTL2_II | 0.791 |
| SSTL15 | 0.780 |
| SSTL2_II_DCI | 1.178 |
| SSTL18_II_DCI | 0.970 |
| SSTL15_DCI | 0.872 |

It has been observed that there is total 33.7% reduction in power dissipation if we shifted from SSTL2_II_DCI logic family to SSTL15 logic family at the frequency of 1MHZ at FPGA of Virtex-6 as shown in Table 2 and Figure 2.

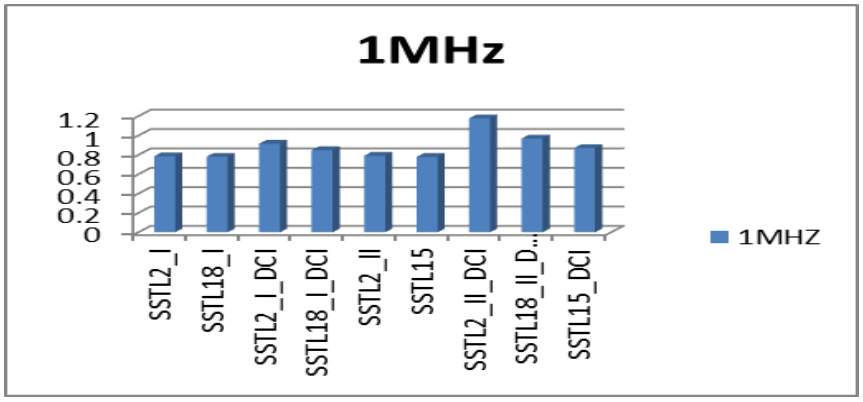


**Figure 2. Total Power Dissipation for Different Logic Families**

- ***Power Dissipation With SSTL Logic at 10 MHz Frequency***

**Table 3. Total Power Dissipation of ISCAS'99 Benchmark Circuits**

| LOGIC FAMILIES | TOTAL POWER DISSIPATION |
|---|---|
| SSTL2_I | 0.786 |
| SSTL18_I | 0.782 |
| SSTL2_I_DCI | 0.916 |
| SSTL18_I_DCI | 0.849 |
| SSTL2_II | 0.791 |
| SSTL15 | 0.780 |
| SSTL2_II_DCI | 1.178 |
| SSTL18_II_DCI | 0.970 |
| SSTL15_DCI | 0.872 |

It has been observed that there is total 33.7% reduction in power dissipation if we shifted from SSTL2_II_DCI logic family to SSTL15 logic family at the frequency of 10 MHZ at FPGA of Virtex-6 as shown in Table 3 and Figure 3.

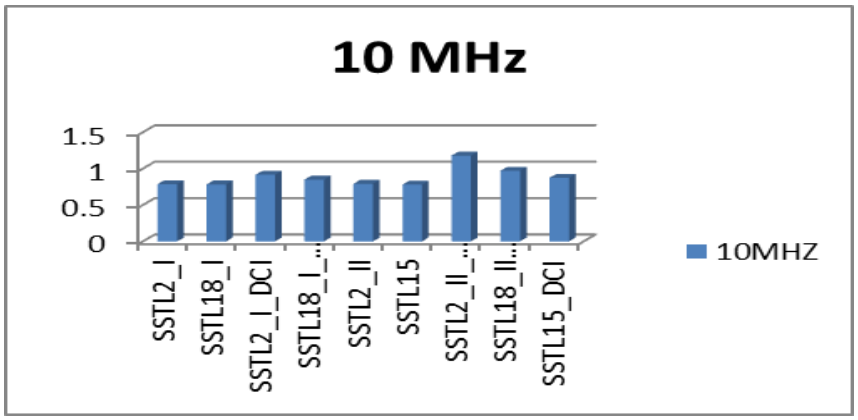


**Figure 3. Total Power Dissipation for Different Logic Families**

- ***Power Dissipation With SSTL Logic at 100MHz Frequency***

**Table 4. Total Power Dissipation for Different Logic Families**

| LOGIC FAMILIES | TOTAL POWER DISSIPATION |
|---|---|
| SSTL2_I | 0.788 |
| SSTL18_I | 0.784 |
| SSTL2_I_DCI | 0.918 |
| SSTL18_I_DCI | 0.851 |
| SSTL2_II | 0.793 |
| SSTL15 | 0.782 |
| SSTL2_II_DCI | 1.178 |
| SSTL18_II_DCI | 0.970 |
| SSTL15_DCI | 0.872 |

It has been observed that there is total 33.6% reduction in power dissipation if we shifted from SSTL2_II_DCI logic family to SSTL15 logic family at the frequency of 100 MHZ at FPGA of Virtex-6 as shown in Table 4 and Figure 4.

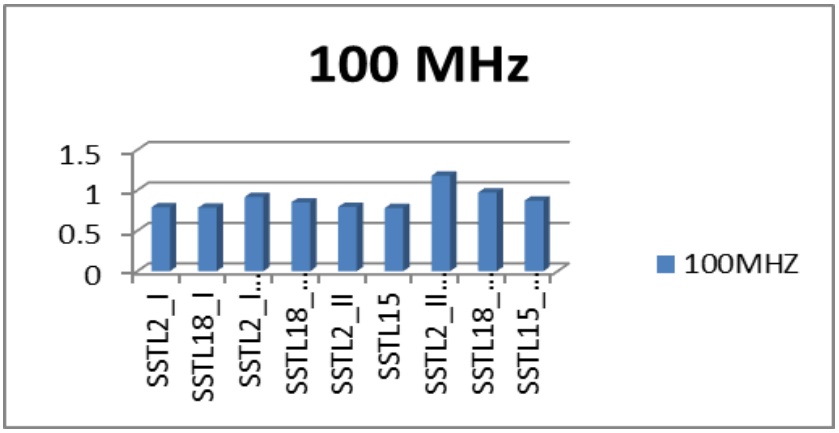


**Figure 4. Total Power Dissipation for Different Logic Families**

- ***Power Dissipation With SSTL Logic at 1 GHz Frequency***

**Table 5. Total Power Dissipation of ISCAS'99 Benchmark Circuits**

| LOGIC FAMILIES | TOTAL POWER DISSIPATION |
|---|---|
| SSTL2_I | 0.810 |
| SSTL18_I | 0.814 |
| SSTL2_I_DCI | 0.939 |
| SSTL18_I_DCI | 0.871 |
| SSTL2_II | 0.817 |
| SSTL15 | 0.803 |
| SSTL2_II_DCI | 1.200 |
| SSTL18_II_DCI | 0.993 |
| SSTL15_DCI | 0.895 |

It has been observed that there is total 33.08% reduction in power dissipation if we shifted from SSTL2_II_DCI logic family to SSTL15 logic family at the frequency of 1GHZ at FPGA of Virtex-6 as shown in Table 5 and Figure 5.

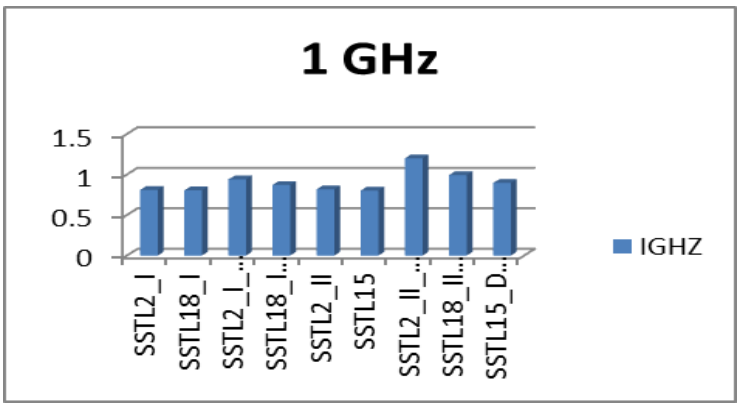


**Figure 5. Total Power Dissipation for Different Logic Families**

- ***Power Dissipation With SSTL Logic at 10 GHz Frequency***

**Table 6. Total Power Dissipation of ISCAS'99 Benchmark Circuits**

| LOGIC FAMILIES | TOTAL POWER DISSIPATION |
|---|---|
| SSTL2_I | 1.02 |
| SSTL18_I | 1.006 |
| SSTL2_I_DCI | 1.144 |
| SSTL18_I_DCI | 1.609 |
| SSTL2_II | 1.049 |
| SSTL15 | 1.012 |
| SSTL2_II_DCI | 1.401 |
| SSTL18_II_DCI | 1.196 |
| SSTL15_DCI | 1.102 |

It has been observed that there is total 27.7% reduction in power dissipation if we shifted from SSTL2_II_DCI logic family to SSTL15 logic family at the frequency of 10GHZ at FPGA of Virtex-6 as shown in Table 6 and Figure 6.

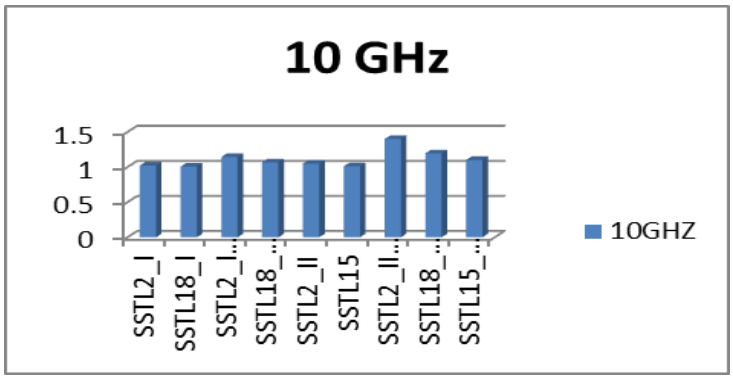


**Figure 6. Total Power Dissipation for Different Logic Families**

- ***Power Dissipation With SSTL Logic at 100GHz Frequency***

**Table 7. Total Power measurement of ISCAS'99 Benchmark Circuit**

| LOGIC FAMILIES | TOTAL POWER DISSIPATION |
|---|---|
| SSTL2_I | 3.117 |
| SSTL18_I | 3.103 |
| SSTL2_I_DCI | 3.185 |
| SSTL18_I_DCI | 3.044 |
| SSTL2_II | 3.373 |
| SSTL15 | 3.008 |
| SSTL2_II_DCI | 3.406 |
| SSTL18_II_DCI | 3.23 |
| SSTL15_DCI | 3.168 |

It has been observed that there is total 11.68% reduction in power dissipation if we shifted from SSTL2_II_DCI logic family to SSTL15 logic family at the frequency of 100GHZ at FPGA of Virtex-6 as shown in Table 7 and Figure 7.

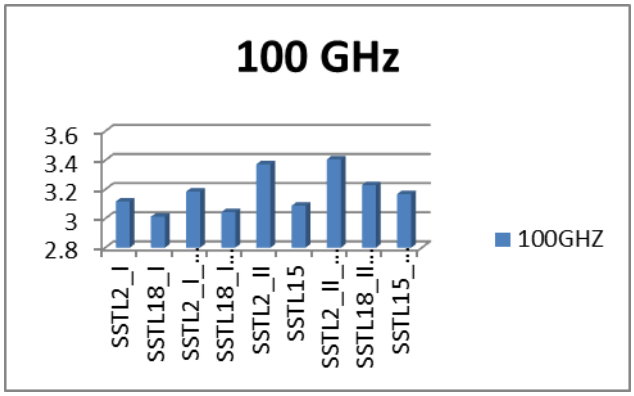


Figure 7: Total Power Dissipation for Different Logic Families

- ***Power Dissipation With SSTL Logic at 1 THz Frequency***

**Table 8: Total Power measurement of ISCAS'99 Benchmark Circuit Design**

| LOGIC FAMILIES | TOTAL POWER DISSIPATION |
|---|---|
| SSTL2_I | 23.836 |
| SSTL18_I | 22.861 |
| SSTL2_I_DCI | 23.364 |
| SSTL18_I_DCI | 22.575 |
| SSTL2_II | 26.291 |
| SSTL15 | 23.608 |
| SSTL2_II_DCI | 23.206 |
| SSTL18_II_DCI | 23.326 |
| SSTL15_DCI | 23.576 |

It has been observed that there is total 14.13% reduction in power dissipation if we shifted from SSTL2_II logic family to SSTL18_I_DCI logic family at the frequency of 1THZ at FPGA of Virtex-6 as shown in Table 8 and Figure 8.

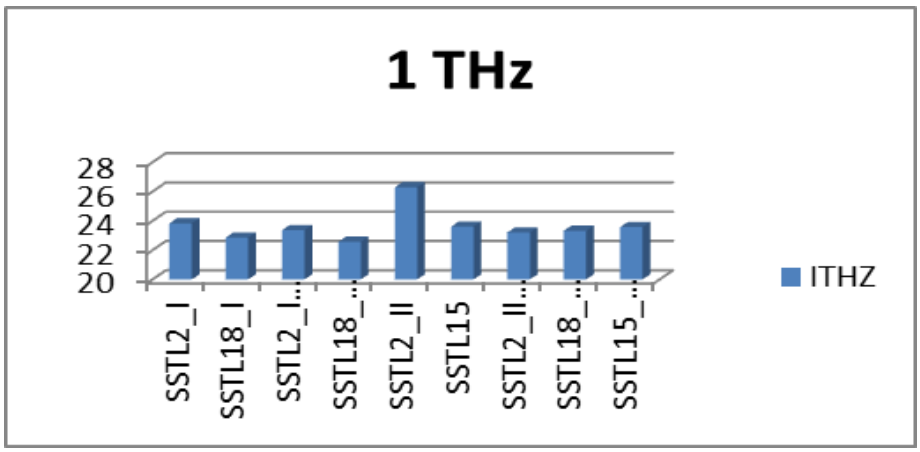


**Figure 8. Total Power Dissipation for Different Logic Families**

## 3. Conclusion

It has been concluded that if we are measuring the clock power, logic power and signals power for different logic families at one frequency then these powers comes out to be the same that concludes that these three powers are same for all the SSTL Logic families for some same frequency but the total power (including clocks, logic, signals, IOs, leakage powers) keeps on changing for different SSTL logic families even at one same frequency. Upto 100GHz of frequency, there will be maximum power dissipation again in case of SSTL2_II_DCI and minimum power dissipation in case of SSTL15 and the power reduction is reduced from 33.7% to 11.68% if we switch from SSTL2_II_DCI logic family to SSTL15 logic family at Virtex-6. At the frequency of 1THZ frequency the maximum power dissipation is in case of SSTL2_II logic family and minimum power dissipation in case of SSTL18_I_DCI and the power reduction is of 14.13% if we move from SSTL2_II logic family to SSTL18_I_DCI logic family at the frequency of 1THz at FPGA of Virtex 6.

## 4. Future Scope

Since now we have worked on Virtex-6 FPGA, we can also implement SSTL based logic families available on Virtex-2, Virtex-3, Virtex-4, Virtex-5 and Virtex-7. We can also implement the different IO standards such as LVMOS, LVDCI, HSTL, LVPECL, Differential LVPECL and many more.

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