International Journal of Bio-Science and Bio-Technology
Vol.8, No.6 (2016), pp. 139-144
http://dx.doi.org/10.14257/ijbsbt.2016.8.6.14

A Modified Architecture for Fingerprint Sensor of Switched Capacitive Integrator Scheme

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Abstract

In this paper, modified architecture of CMOS capacitive fingerprint sensor readout circuit is presented for general type of a switched capacitive integrator scheme. The proposed architecture supports wide and flexible operation range without ADC. It also operates faster than a typical integrator scheme for one frame image capture. The circuit includes an analog comparator in each pixel and counters. The referenced analog voltage of each sensor cell is controlled by an external or internal bias.

Keywords*: Switched Capacitor, Integrator, Fingerprint Sensor Readout Scheme, Parasitic Insensitive, Comparator*

1. Introduction

Currently, the convenience of appliances like mobile phones, IC cards, and notebook computers brings us better life. The demand for user authentication is becoming more and more important. Biometric recognition systems, such as a fingerprint system, are for personal verification. A fingerprint system or other biometric systems have not been popular in the consumer market due to its inconvenience for use and relatively high cost. Fingerprint solution on mobile phone has been got a lot of attention recently as Apple released iPhone6s. Fingerprint sensor can benefit in both on high level of security and also user convenience [1-3]. Since a biometric sensor needs to sense very small capacitance variation formed between a fingerprint and a sensor plate, it is more important to control the effects from parasitic components. Therefore, the effect of parasitic capacitances formed inevitably from the structure of the sensor cell should be removed for accurate sensing. Many fingerprint sensors based on capacitive sensing has been proposed already. Figure 1 shows a conventional fingerprint senor structure using a switched integrator scheme. A switched capacitive integrator scheme is effective in respect of low noise and sensing performance. A capacitive sensor based on charge transfer circuit has also been proposed [4-7]. An integrator based on an AOVF charge transfer circuit for capacitive sensing to get large output sensing range of capacitive sensing has been proposed [8]. Since this circuit combines a passive integrator and a parasitic-insensitive discrete-time integrator, the circuit can use the capacitive sensing range of full supply voltage, which is suitable for low voltage and low power applications. But, these switched capacitive integrator schemes need a full integration time and complicated circuits like pipelined sensing for reducing image capture time.

This paper proposes the modified architecture of CMOS capacitive fingerprint sensor readout circuit for a general or specific type of a switched capacitive integrator scheme. The proposed architecture supports wide and flexible operation range without ADC (analog to digital converter).

ISSN: 2233-7849 IJBSBT

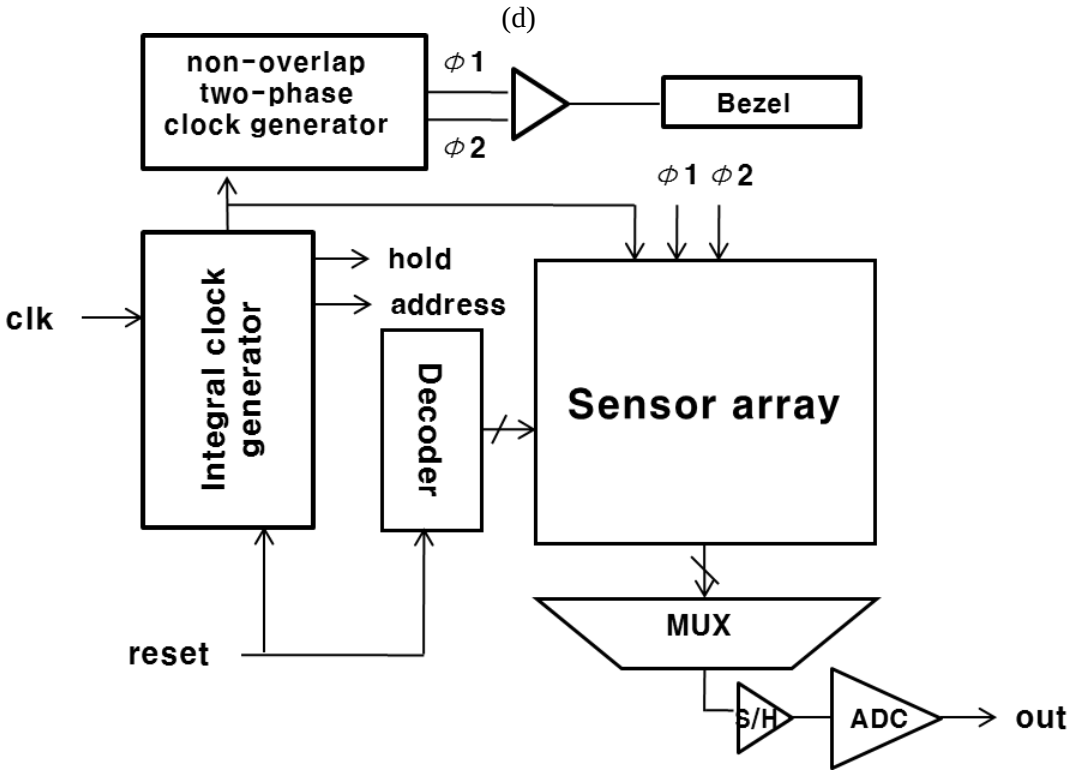
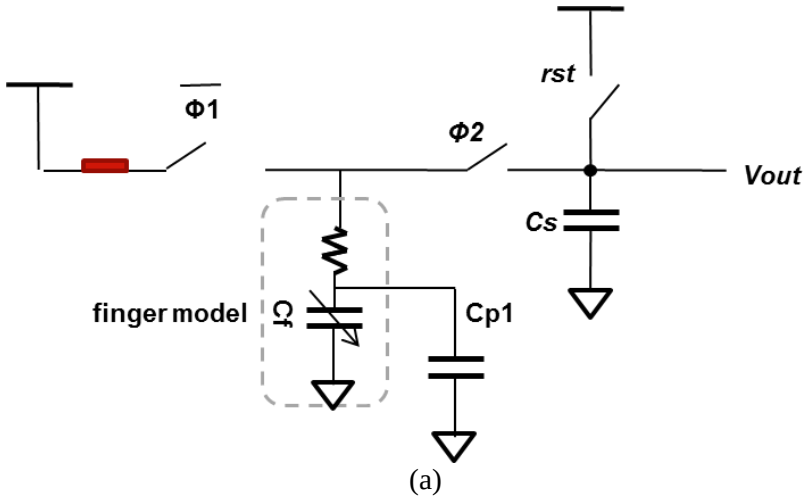


Figure 1. Conventional Fingerprint Senor Structure for a Switched Integrator Scheme

2. Switched Capacitor Charge Integrator Scheme

Capacitive sensors based on switched capacitor charge integrator scheme have been presented [4-8]. Four types of capacitive sensors based on charge integrator, are compared as shown in figure 2. A passive charge transfer circuit is shown in figure 1(a). A discrete-time charge integrator based on switched-capacitor integrator as a capacitive sensor is shown in Figure 1(b). A parasitic-insensitive charge integrator which reduces the non-ideal affects generated from parasitic resistor and capacitor is shown in figure 1(c). A parasitic-insensitive charge integrator circuit with active output voltage feedback to get large output sensing range of capacitive sensing is shown in figure 1(c).



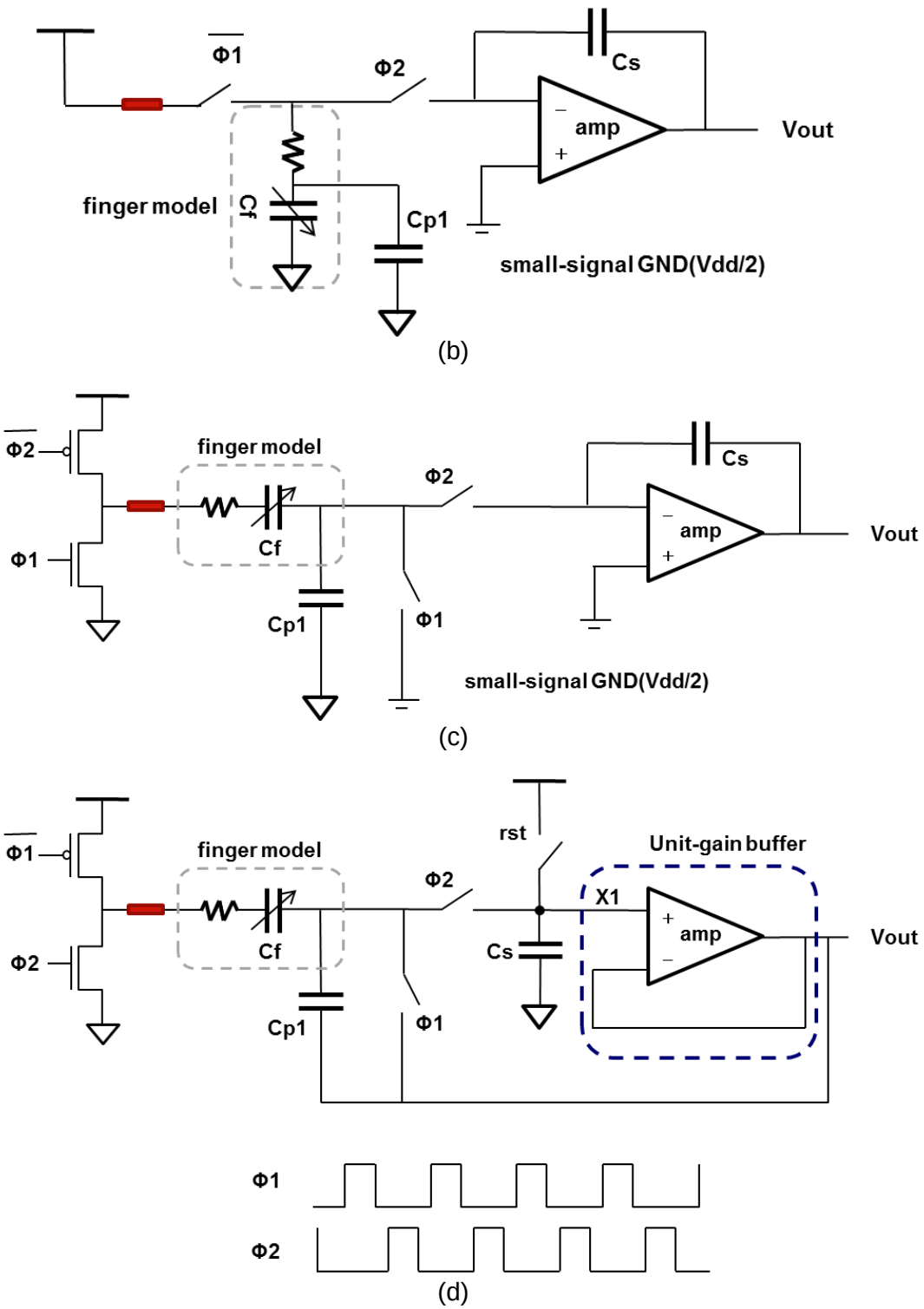


Figure 2. Capacitive Sensors Based on Switched Capacitor Charge Integrator Circuit

(a) sensor based on passive charge transfer circuit (b) sensor based on parasitic-sensitive discrete-time integrator (c) sensor based on parasitic-insensitive discrete-time integrator (d) sensor based on passive-style charge transfer with active output voltage feedback

The clock signals, Φ1 and Φ2, are non-overlap control signal. A figure 2(a) sensor based on a passive charge integrator, has two switches and capacitors, Cf and Cs. The two switches are controlled by non-overlapping two phase clocks. Note that a resistor can be effectively replaced by a capacitor with switches in clocked systems. Therefore, the charge transfer is similar that of a RC scheme. The output is saturated as the voltage goes up. The charges of Cf are redistributed and shares with Cs at ϕ2, and the variation for a single transition depends on the previous output. Figure 2(b) shows a capacitive sensor circuit based on discrete-time integrator. The circuit can increase the linearity of charge transfer, which improves sensitivity. Since positive input of amp maintains AC ground. A parasitic capacitor, Cp also stores charges during the ϕ1 phase and affects to output during the ϕ1 phase. In a wider array sensor, the larger parasitic components may affect the performance degradation of capacitive sensitivity. To improve performance, parasitic insensitive charge transfer circuit based on discrete-time integrator as shown in figure 2(c) can be presented. It can decrease the non-ideal effect caused from the parasitic components in capacitive sensor. Cp is charged to small-signal ground during the ϕ1 phase so that there are no charges from the parasitic capacitor formed in the sensor line during the ϕ2 evaluation phase. The parasitic insensitive charge transfer circuit does not transfer charges from parasitic capacitors as well as linear charge transition. To increase the output range, a passive-style charge transfer circuit with active output voltage feedback for capacitive sensing has been proposed. To increase output sensing voltage range, this circuit combines a passive integrator and a parasitic-insensitive discrete-time integrator as shown in figure 2(d). The circuit has passive and the parasitic-insensitive integrator circuits. It uses the same MOS switch topologies of a parasitic-insensitive discrete-time integrator. Therefore, the output range is the same with passive integrator, which is full supply range. This circuit also has a linear charge transfer characteristic as a discrete-time integrator does by balancing the same voltage before charge transfer using active output voltage feedback shown in figure 2(d). The parasitic capacitance does not affect the charge transfer to the output. Figure 3 shows a typical timing operation at a ridge and valley of a switched capacitor charge integrator circuit. T1 is destination time of ridge and T2 is for valley.

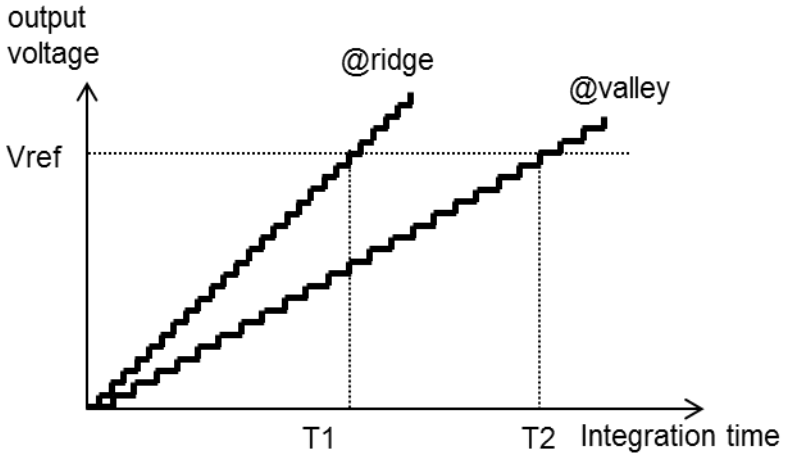


Figure 3. Typical Timing Operation at a Ridge, Valley of one Pixel

3. Modified Sensing Scheme

Typical charge integrator sensing scheme needs a complicated circuit including ADC and long time for an image capture of one frame as shown in figure 2 and 3. Figure 4 shows the modified charge integrator sensing architecture. Each pixel is composed with a switched capacitor integrator block, counters for detecting a ridge or valley and analog comparator. T1 and T2 are used for disable signal of each counter. When the c_out is triggered, the counter does not operate. T1 is faster than T2 as shown in figure 3. Because the final value of counter is different in valley and ridge, the proposed circuit does not ADC any more. The counter value of each sensor pixel is a gray scale image. . The proposed architecture supports wide and flexible operation range without ADC by calibrating the Vref signal. It also operates faster than a typical integrator scheme. The circuit includes an analog comparator in each pixel and 8 bit registers. The referenced analog voltage of each sensor cell is controlled by an external or internal bias.

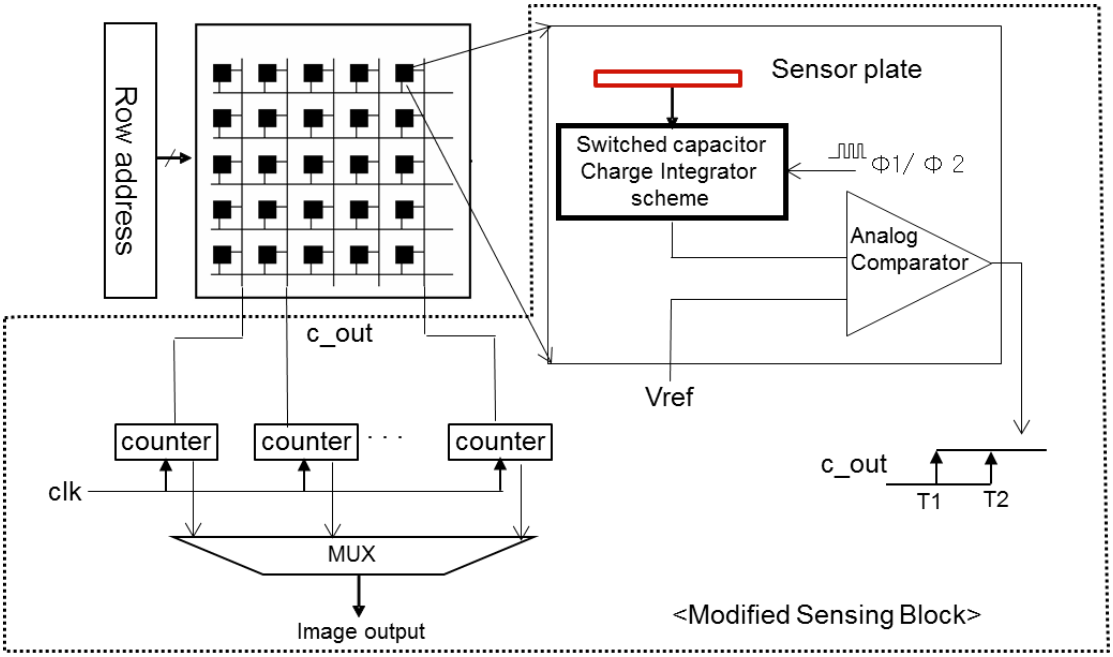


Figure 4. Proposed Modified Charge Integrator Sensing Architecture

4. Conclusion

This paper introduces the modified architecture of CMOS capacitive fingerprint sensor readout circuit for a general or specific type of a switched capacitive integrator scheme. A switched capacitive integrator scheme is effective in respect of low noise and sensing performance. But, typical charge integrator sensing scheme needs a complicated circuit including ADC and long time for an image capture of one frame. Each pixel of modified circuit is composed with a switched capacitor integrator block, counter and analog comparator. Because the final value of counter is different in valley and ridge, the proposed circuit does not ADC any more. The counter value of each sensor pixel is a gray scale image. . The proposed architecture supports wide and flexible operation range without ADC. It also operates faster than a typical integrator scheme. The circuit includes an analog comparator in each pixel and 8 bit registers.

Acknowledgements

This work was supported by Hanshin University Research Grant.

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