

Design and Implementation of Fingerprint Sensor for Calibration of Parasitic Offset Image

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Abstract

A FPGA implementation of fingerprint sensors scheme is described for removing parasitic offset image on no touch. This paper proposes an effective fingerprint identification system with 160x192 array fingerprint sensor hardware. The proposed calibration scheme initializes a fingerprint sensor LSI to eliminate the influence of offset image by the electrical characteristic difference of pixel array, which is degraded during long-time use. Each step of a fingerprint algorithm is analyzed based on FPGA. This paper designs an effective hardware scheme for using the Verilog-HDL in 160x192 pixel array. The circuit includes 3 memories and control logic. The function is verified in RTL simulation and FPGA logic synthesis.

Keywords: *Offset image, Fingerprint Sensor, Cell array, FPGA, RTL Synthesis*

1. Introduction

The fact that fingerprints are unique to each person has been well established. The recent expansion of trading by internet, smart phone system and the needs to prevent unauthorized usage of private communication and information processing systems open new opportunities to authentication systems. In that sense, a portable fingerprint recognition system, especially a silicon-based sensor system could be an ideal candidate [1-6]. Fingerprint is a collection of ridge and valley patterns of human's fingertip and has its own unique characteristics, that enables each individuals to differentiate from others. The uniqueness of a fingerprint is exclusively determined by the local ridge characteristics and their relationships. From partial characteristics, the most important and considerable ridge characteristics are called minutiae, and amongst them, there are ridge ending and ridge bifurcation. A ridge ending is defined as the point where a ridge ends abruptly. Since the surface of a fingerprint sensor is exposed to capture a fingerprint image by finger touching, the condition of the sensor surface changes during long-term use. In other words, the sensor surface becomes dirty in practical use[7]. The image of fingerprint sensor is also distorted from electrical characteristic difference of each pixel on a sensor array. Gradually, a parasitic capacitance is formed between the dirt and the sensor plate, and the sensed capacitance increases as a result. This means that the output signal from the fingerprint sensor depends on the sensor surface condition and electrical characteristic difference of each pixel on a sensor array. Thus, the change of the surface condition degrades the captured fingerprint images. The degraded fingerprint images make accurate user authentication impossible. To achieve accurate authentication, the fingerprint sensor has to capture clear fingerprint images even though the sensor surface condition has changed. Conventional fingerprint sensors have no circuit technique that addresses this issue. To solve this problem, we propose a pixel-level automatic calibration circuit. This paper describes the pixel-level automatic calibration circuit scheme, which

initializes the sensing characteristics and eliminates the influence of the sensor surface condition.

2. Calibration Scheme

There are some calibration schemes for fingerprint image enhancement from many causes [6-7]. A fingerprint image may be corrupted by dirty materials or electrical characteristic differences of each sensor pixel. The simple method is calibration by DAC (digital to analog converter) for removing the influence of dirty materials [7]. Sensor array block shows the horizontal and vertical array of each sensor pixel in figure 1. DAC receives digital input from an external CPU to create a reference voltage, an average voltage of ridge and valley, as an output. A referenced voltage compares the voltage from the sensor and fingerprint's ridge and valley to create binary image. This method swings a reference voltage from 0 volt to VDD, at an initial fingerprint sensor operation, without contacting a fingerprint, to find optimum ridge and valley voltage. This method is to adapt to changes in reference voltage due to contamination from an initial fingerprint as well as a variation in process. However, its layout area is very big and complex in general, and need to use a high performance DAC. Therefore, installation within each sensor pixel is impossible, thus application of multiple outer DAC is necessary. Furthermore, this could create differences in DAC characteristics and qualities of image in pixel domain. Moreover, DAC's power consumption is dominant problem. The critical problem is that it is not easy to integrate a sensor and the DAC on a chip.

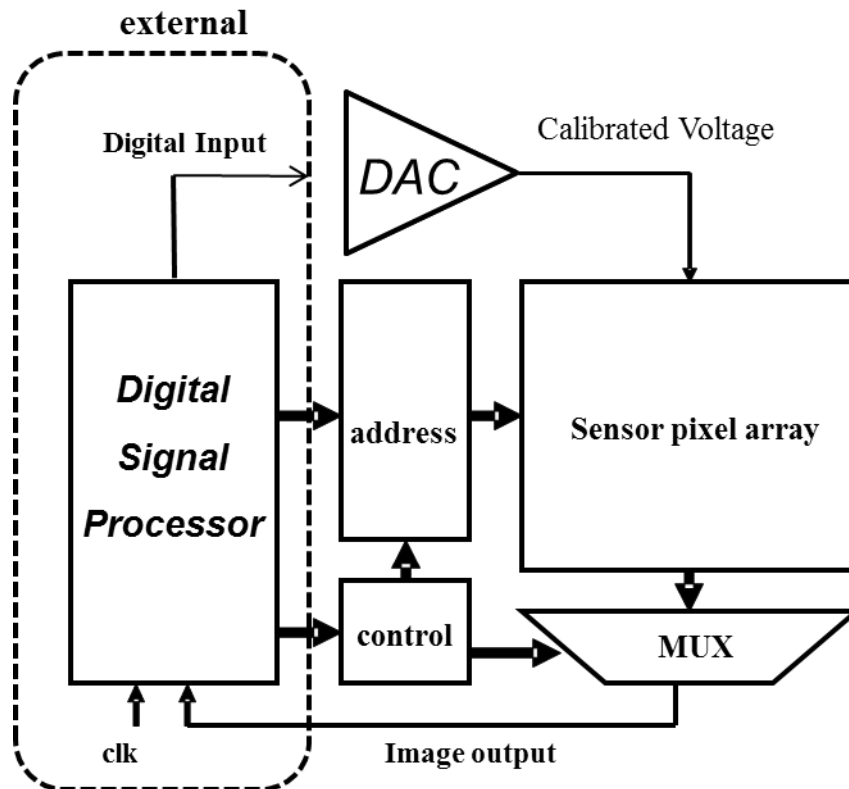


Figure 1. Typical Calibration Scheme for Fingerprint Image Enhancement

The better solution will be to embed a compensation circuit into an individual sensor pixel as shown in figure 2. This method applies a charge pump circuit for a pixel-level auto calibration scheme [7-8]. In general, a charge pump circuit is applied as a voltage multiplier for a nonvolatile memory. Due to non-overlapping two clock signals $\phi 1$ and $\phi 2$, a voltage gradually increases. One stage is comprised of one diode and actual coupling capacitor. As an effect of diode the voltage is transferred to only one direction, to show an overall gradual output voltage increase effect. This increased voltage is applied as a comparator's reference voltage. The comparator compares the reference and the sensor voltage then, decides whether the image is a ridge or valley. In order to apply charge pump circuit to fingerprint's each pixel, there are few optimization. In order to achieve these optimizations, we determined the number of diode-capacitor pairs stage to make layout possible within limited sensor pixel areas. In addition, since there is a limitation in a pixel area to apply actual capacitor as an active layer and poly or metal layer, all capacitors are implemented as MOS transistors.

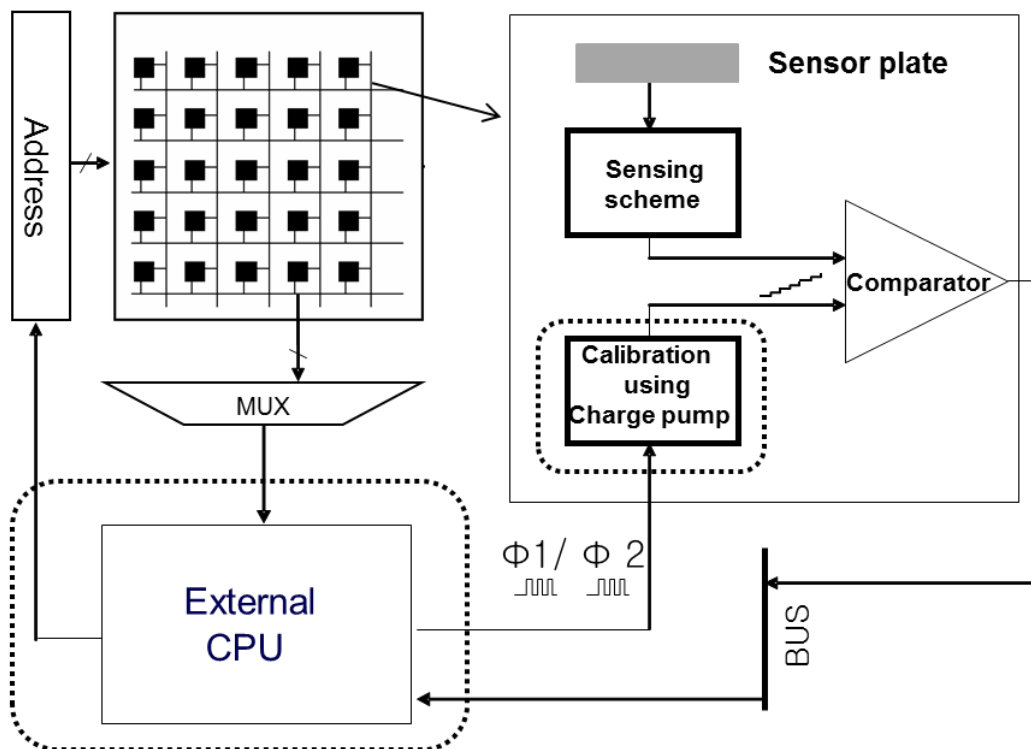


Figure 2. Pixel-Level Automatic Calibration Circuit Scheme

3. Proposed Calibration Structure and FPGA Implementation

This paper proposes a fingerprint detection hardware scheme to calibrate a sensor surface image with finger removing the electrical characteristic difference of each pixel. This paper proposes the operation algorithm using a memory block. The left picture shows initial sensor operation. Without a finger contact, the image is only sensor surface image without finger by electrical characteristic difference of each pixel. It then saves to memory 1. The right picture in picture 3 shows normal operation of fingerprint contact. It then saves to memory 2 and the image is normal sensor surface image with finger including electrical characteristic difference of

each pixel. The microcontroller compares a fingerprint's image of memory1 and memory2. Finally, microcontroller subtracts memory2 from each pixel's offset image of memroy1, to acquire a compensated value, which is a corrected image, without initial distorted image. The image is calibrated sensor surface image with finger removing the electrical characteristic difference of each pixel. If the area of chip is not sufficient, then we may not use memroy3 by double using of memory2.

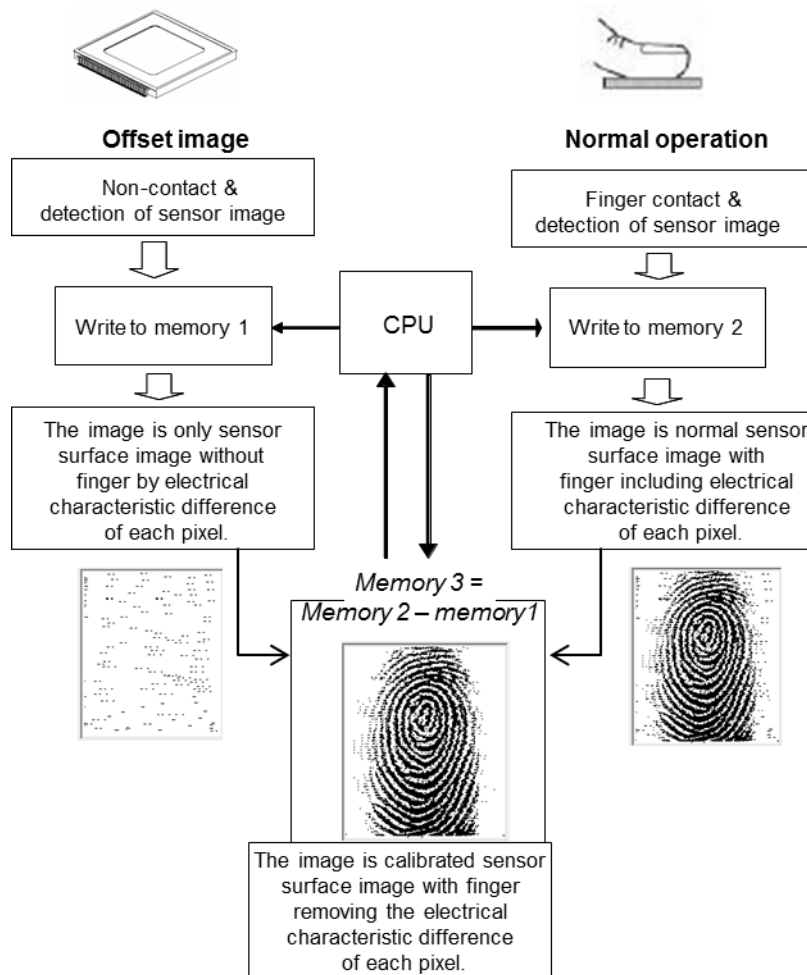


Figure 3. Proposed Calibration Scenario

Figure 4 shows the circuit block diagram of the proposed area type fingerprint sensor with 192 x 160 pixels. The offset image is captured during cycle 1 and writes to memory 1 at the same time. The image is only sensor surface image without finger by electrical characteristic difference of each pixel. In cycle 2, the normal image is captured and the image is calibrated sensor surface image with finger removing the electrical characteristic difference of each pixel. If the area of chip is not sufficient, then we may not use memroy3 by double using of memory2. The circuit subtracts memory2 from each pixel's offset image of memroy1 and writes to memory 3. The image is calibrated sensor surface image with finger removing the electrical characteristic difference of each pixel. For SPI communication, the circuit applies SPI controller block using parallel to serial register, so the output signal 'sdout' is serial data output. The figure 5 shows logic simulation result and figure 6 is synthesized schematic from FPGA environment. Selected device of FPGA is Xilinx 4vlx200ff1513-12. As a result of logic synthesis, number of slices are 209. Slice flip flops are 185, number of 4 input LUTs are 364 and FIFO16/RAMB16s are 15.

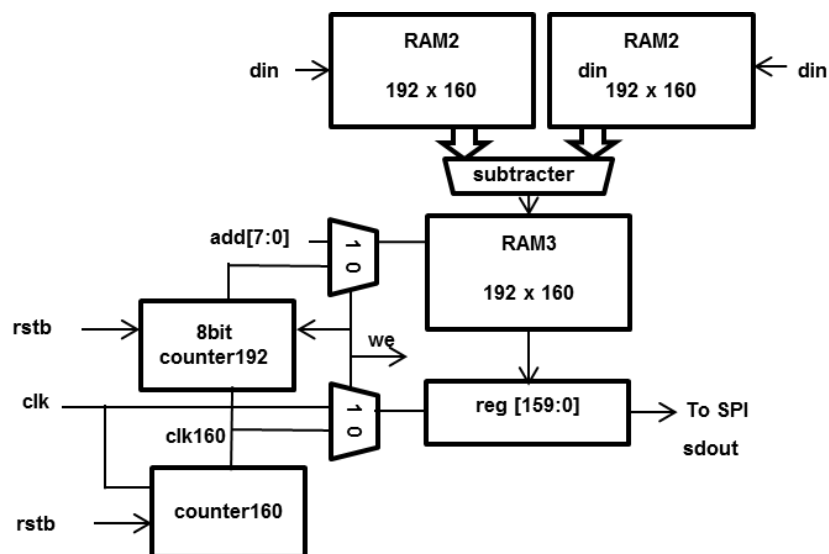
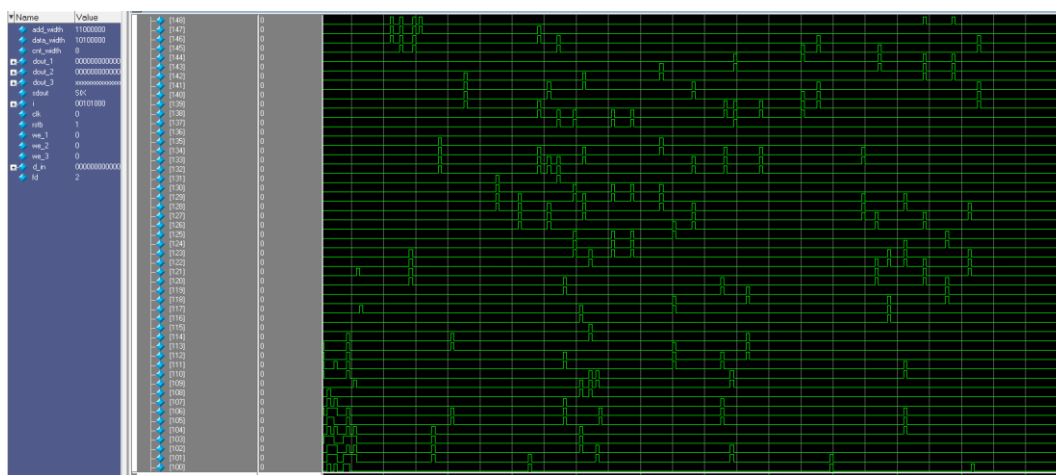
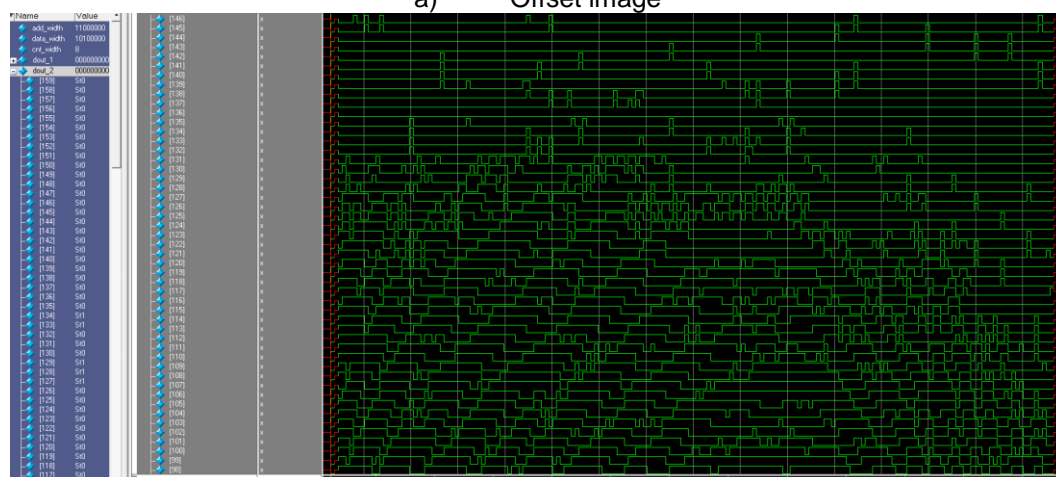
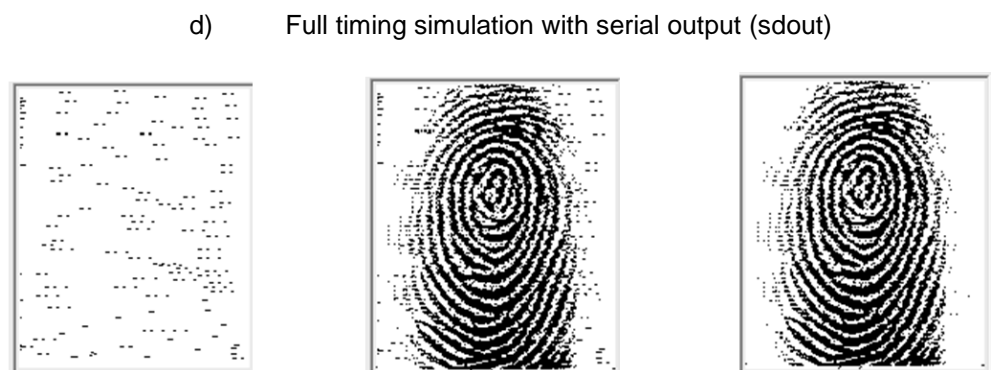
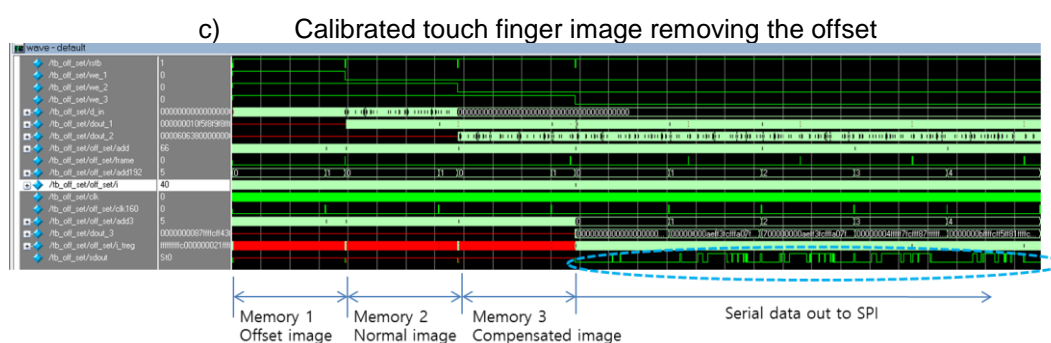
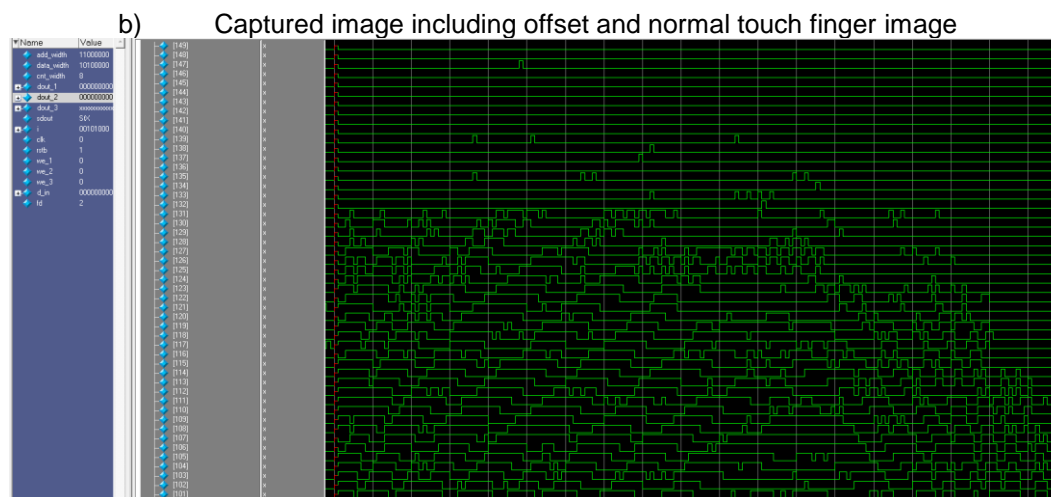


Figure 4. Circuit Architecture



a) Offset image





Sample offset image touch image with offset compensated image

e) Result of image processing on FPGA

Figure 5. Simulation Results of Fingerprint LSI

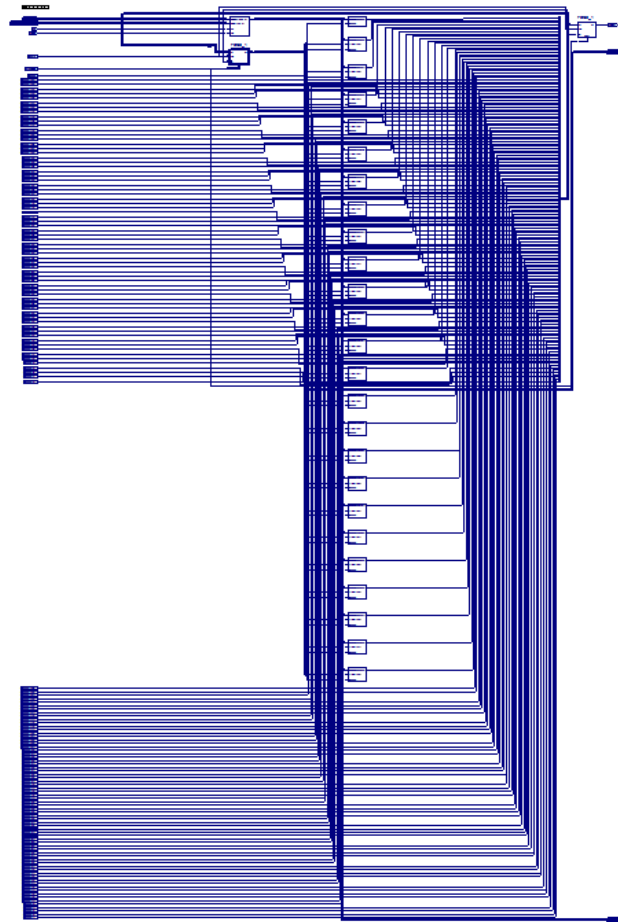


Figure 6. Logic synthesis result of FPGA

4. Conclusion

This paper proposes a fingerprint detection hardware scheme to calibrate a sensor surface image with finger removing the electrical characteristic difference of each pixel. This paper proposes the operation algorithm using a memory block. A FPGA implementation of fingerprint sensors scheme is described for removing parasitic offset image on no touch. This paper proposes an effective fingerprint identification system with 160x192 array fingerprint sensor hardware. The proposed calibration scheme initializes a fingerprint sensor LSI to eliminate the influence of offset image by the electrical characteristic of a cell array, which is degraded during long-time use. Each step of a fingerprint algorithm is analyzed based on FPGA. This paper designs an effective hardware scheme for using the Verilog-HDL in 160x192 pixel array. The circuit includes 3 memory and control logic. The function is verified in RTL simulation and FPGA logic synthesis. Selected device of FPGA is Xilinx 4vlx200ff1513-12. As a result of logic synthesis, number of slices are 209. Slice flip flops are 185, number of 4 input LUTs are 364 and FIFO16/RAMB16s are 15.

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References

- [1] S. Jung, "A VLSI Implementation of High Sensitive Fingerprint Sensor using Parasitic Insensitive Charge Transfer Circuit," International Journal of Smart Home, vol. 9, no. 7, (2015).
- [2] S. M. Jung, J. M. Nam, D. H. Yang and M. K. Lee, "A CMOS integrated capacitive fingerprint sensor with 32-bit RISC microcontroller," IEEE Journal of Solid-State Circuits, vol. 40, (2005), pp. 1745-1750.
- [3] H. Yeo, "A New Fingerprint Sensor based on Signal Integration Scheme using Charge Transfer Circuit", International Journal of Bio-Science and Bio-Technology(IJBSBT), vol. 7, no. 1, (2015), pp. 29-38,
- [4] S. M. Jung, "Active Capacitive-Sensing Circuit Technique for Image Quality Improvement on Fingerprint Sensor," Journal of Next Generation Information Technology (JNIT), vol. 4, no. 3, (2013), pp. 47-53.
- [5] S. M. Jung, "An Implementation of Parasitic Insensitive 128 x100 Pixels Fingerprint Sensor using Modified Switched Capacitor Integrator", International Journal of Bio-Science and Bio-Technology(IJBSBT), vol. 6, no. 6, (2014), pp. 121-128.
- [6] J. M. Nam, S. M. Jung and M. K. Lee, "Design and implementation of a capacitive fingerprint sensor circuit in CMOS technology", Sensors and Actuators a Physical, vol. 135, iss. 1, (2007).
- [7] H. Morimura, S. Shigematsu, T. Shimamura, K. Machida and H. Kyuragi , "A Pixel-Level Automatic Calibration Circuit Scheme for Capacitive Fingerprint Sensor LSIs , IEEE J. of Solid-state circuits, vol. 37, no. 10, (2002), pp 1300-1306.

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