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Capacitance Scaling With Different IO Standard Based Energy Efficient Bio-Medical Wrist Watch Design on 28nm FGPA

Shivani Madhok[1], Gaurav Verma[2], Ankur Bhardwa[3]j, Himanshu Verma[4], Ipsita Singh[5], Sushant Shekhar[6]

[1]*Chitkara University Research and Innovation Network*
Chitkara University, Chandigarh, Punjab Department of ECE
[2,3,4,5,6]*Jaypee Institute of Information Technology*
Noida, India
shivanimadhok0@gmail.com

Abstract

In this paper, we have designed an energy efficient wrist watch on 28nm FPGA. The code has been implemented in Xilinx ISE Design Suite 14.2. The device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. The wrist band will take the blood pressure as input and will tell about the state of the person wearing it. The design supports Internet of things service that's why IP addresses are involved. This wrist band design is very helpful in biomedical areas. Research is in progress in this field. In this paper frequency is varied to obtain power consumption of Wrist Watch. Airflow has been kept 250 LFM and medium Heat sink. IO Standards has been varied in order to achieve an energy efficient device. Main emphasis has been done on MOBILE_DDR, LVTTL, HSUL_12, HSTL_I, LVCMOS33 and SSTL15 IO Standards. To design an energy efficient device we are using capacitance scaling and the capacitance is scaled down from 100pF to 20pF. During capacitance scaling, we observe that there is no change in clock power, logic power and signal power. Thermal Aware design is current research area. Analysis has been at two temperatures that is at 25 degree Celsius and at 50 degree Celsius. At the end we can conclude that the maximum power is consumed at 2.2GHz and minimum power is consumed at 1.2GHz. In respect of capacitance maximum power is consumed at 100pF and minimum power is consumed at 20pF at both temperatures at 25 degree Celsius and 50 degree Celsius.

Keywords*: Capacitance, FPGA, energy efficient, IO Standard, wrist watch*

1. Introduction

In this research work, we have designed a smart wrist band. This wrist band will take the blood pressure as input and will tell about the state of the person wearing it. The outputs can be any as shown in Figure 1 like desired, Hypertensive Emergency, Hypotension, Pre-Hypertension, State1 Hypertension, State2 Hypertension. The design supports Internet of things service that's why IP addresses are involved. The schematic of Wrist Band is shown in Figure 2. The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. All our work is done on 28nm FPGA Kintex-7. The device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. This wrist band design is very helpful in biomedical areas. Research is in progress in this field. Wrist band pulse oximeter has been designed [8]. The wrist band shaped capacitively-coupled electrodes have been developed [9].Wrist band based on custom made antenna for passive NFC tag had been designed [10]. Power analysis has been done at different frequencies mentioned in Table 1. For Image Inverter

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frequency scaling has been done that resulted in variations in power consumption and the Junction temperature [3].

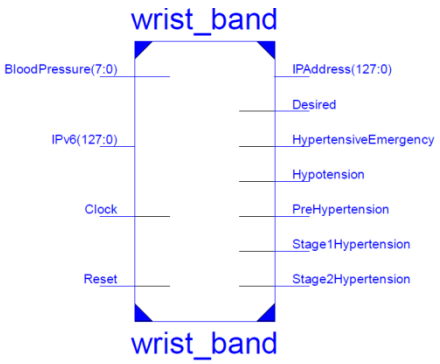

Figure 1. Symbol of Wrist Band

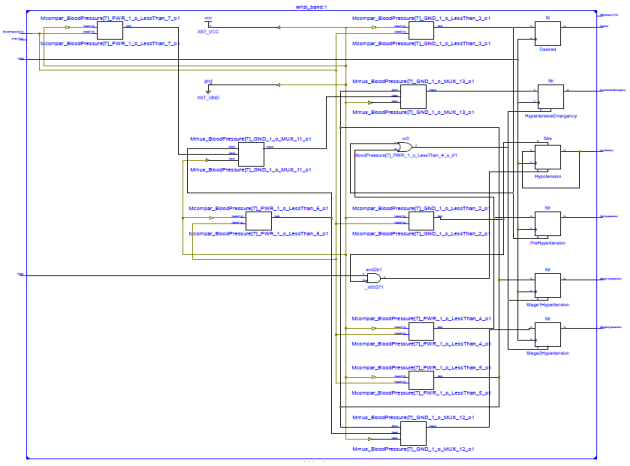

Figure 2. Schematic of Wrist Band

Table 1. Set of Frequencies Taken in Consideration

Frequency	**Mobile set**
1400MHz	Nokia Lumia 710
1.2GHz	Samsung Galaxy Core
2100MHz	I phone6
1700MHz	HTC/T
1800MHz	Micromax X091
2.2GHz	Sony Xperia Z1

In this paper frequency is varied to obtain power consumption of Wrist Watch. Airflow and heat sink are main parameters while analyzing the thermal dissipation in the circuit [1]. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink. IO Standards has been varied in order to achieve an energy efficient device. Main emphasis has been done on MOBILE_DDR, LVTTL, HSUL_12, HSTL_I, LVCMOS33 and SSTL15 IO Standards. Low voltage Transistor-transistor logic (LVTTL) IO standard is used in this design to make it power optimized [11]. HSTL (High Speed Transceiver Logic) and I/O standard is used to make this design more energy efficient [12]. SSTL (Symmetrical Structure Transient Limiter) is widely used for suppressing capacitor switching transients [13].In order to make energy

efficient filter, we are using capacitance scaling [2].To design an energy efficient device we are using capacitance scaling and the capacitance is scaled down from 100pF to 20pF. Clock Power and Signal Power are independent of capacitance scaling [7]. During capacitance scaling, we observe that there is no change in clock power, logic power and signal power.

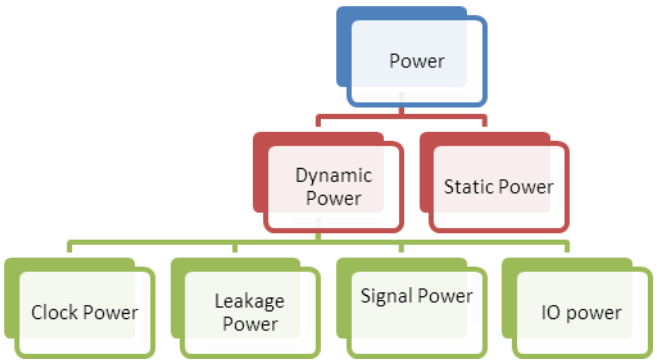

Figure 3. Types of Power

Power is of 2 types: Dynamic power (ON state power) and Static power (OFF state power). Dynamic power or total on-state power is further classified as Clock power, Leakage power, Signal power, IO power as shown in Figure 3 and Figure 4. Analysis has been at two temperatures that is at 25 degree Celsius and at 50 degree Celsius. Thermal Aware design is current research area. There is already work is going on in thermal aware design of FIR Filter [4], thermal aware Key Generator in Green Communication [5] and design of thermal aware ROM [6].

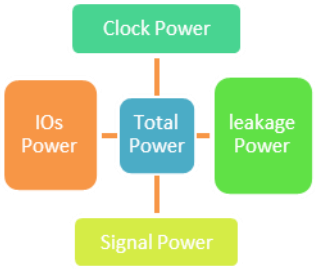

Figure 4: Dynamic Power's Classification

5. Power Analysis

A. Power Analysis for 1400 MHz Frequency

Table 2. Power Analysis at 25°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.208	0.228	0.248	0.269	0.289
LVTTL	0.828	1.323	1.818	2.313	2.809
HSUL_12	0.166	0.173	0.181	0.189	0.196
HSTL_I	0.192	0.203	0.214	0.225	0.236
LVCMOS33	0.828	1.323	1.818	2.313	2.809
SSTL15	0.154	0.157	0.159	0.162	0.165

There is 28.02% reduction in total power dissipation with MOBILE_DDR , 70.52% with LVTTL, 15.30% with HSUL_12, 18.64% with HSTL_I , 70.52% with LVCMOS33 , 6.66% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 2 and Figure 5.

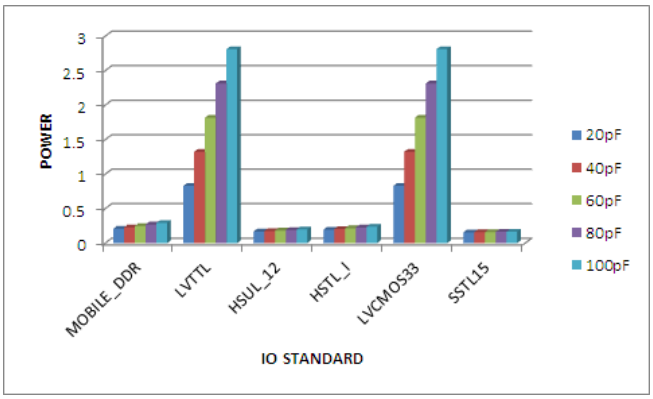

Figure 5: Power Dissipation at 25°Celsius Temperature for 1400 MHz

Table 3. Power Analysis at 50°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.252	0.272	0.292	0.312	0.333
LVTTL	0.874	1.371	1.868	2.366	2.863
HSUL_12	0.209	0.217	0.224	0.232	0.240
HSTL_I	0.235	0.247	0.258	0.269	0.280
LVCMOS33	0.874	1.371	1.868	2.366	2.863
SSTL15	0.197	0.200	0.203	0.206	0.209

There is 24.32% reduction in total power dissipation with MOBILE_DDR , 69.47% with LVTTL, 12.91% with HSUL_12, 16.07% with HSTL_I , 69.47% with LVCMOS33 , 5.74% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 3 and Figure 6.

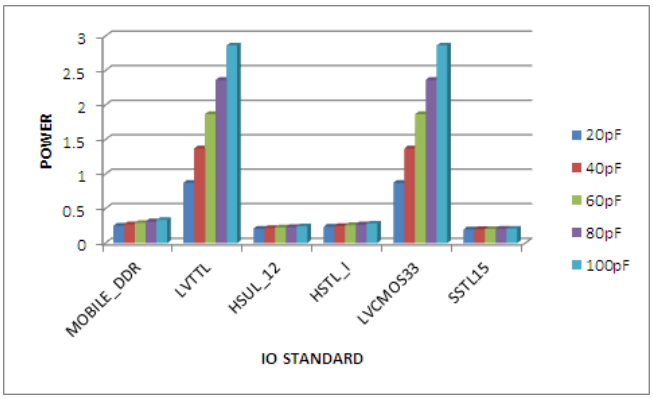

Figure 6. Power Dissipation at 50°Celsius Temperature for 1400 MHz

B. Power Analysis for 1.2 GHz Frequency

Table 4. Power Analysis at 25°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.173	0.188	0.202	0.217	0.232
LVTTL	0.628	0.996	1.363	1.731	2.099
HSUL_12	0.145	0.150	0.156	0.162	0.167
HSTL_I	0.166	0.174	0.182	0.190	0.199
LVCMOS33	0.628	0.996	1.363	1.731	2.099
SSTL15	0.136	0.138	0.140	0.142	0.145

There is 25.43% reduction in total power dissipation with MOBILE_DDR , 70.08% with LVTTL, 13.17% with HSUL_12, 16.58% with HSTL_I , 70.08% with LVCMOS33 , 6.20% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 4 and Figure 7.

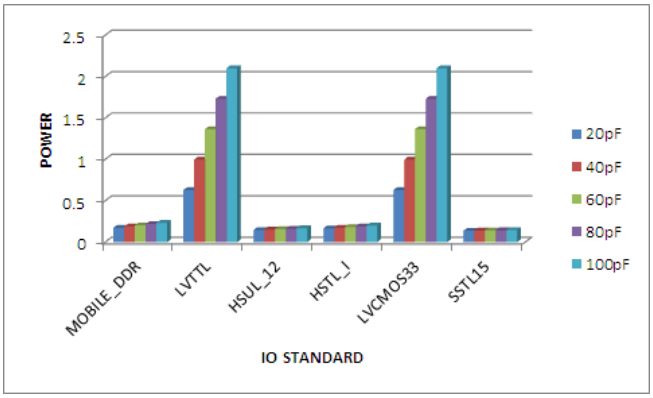

Figure 7. Power Dissipation at 25°Celsius Temperature for 1.2 GHz

Table 5. Power Analysis at 50°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.216	0.231	0.246	0.261	0.276
LVTTL	0.674	1.043	1.412	1.781	2.150
HSUL_12	0.188	0.194	0.199	0.205	0.211
HSTL_I	0.209	0.217	0.226	0.234	0.242
LVCMOS33	0.674	1.043	1.412	1.781	2.150
SSTL15	0.180	0.182	0.184	0.186	0.188

There is 21.73% reduction in total power dissipation with MOBILE_DDR , 68.65% with LVTTL, 10.90% with HSUL_12, 13.63% with HSTL_I , 68.65% with LVCMOS33 , 4.25% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 5 and Figure 8.

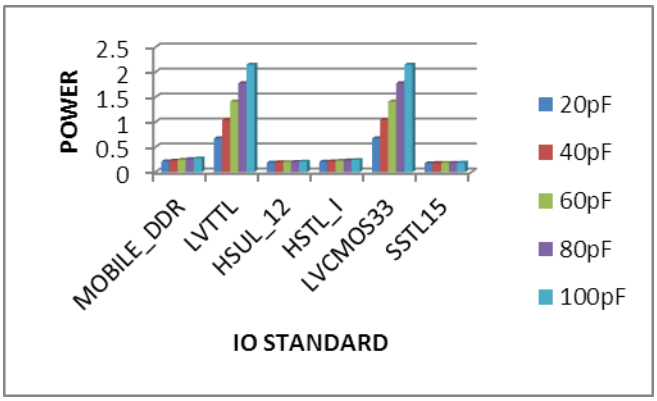

Figure 8. Power Dissipation at 50°Celsius Temperature for 1.2 GHz

C. Power Analysis for 2100 MHz Frequency

Table 6. Power Analysis at 25°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.372	0.417	0.461	0.505	0.549
LVTTL	1.756	2.847	3.939	5.030	6.122
HSUL_12	0.216	0.278	0.294	0.311	0.328
HSTL_I	0.311	0.335	0.360	0.384	0.409
LVCMOS33	1.756	2.847	3.939	5.030	6.122
SSTL15	0.233	0.239	0.245	0.251	0.258

There is 32.24% reduction in total power dissipation with MOBILE_DDR , 71.31% with LVTTL, 15.30% with HSUL_12, 23.96% with HSTL_I , 71.31% with LVCMOS33 , 9.68% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 6 and Figure 9.

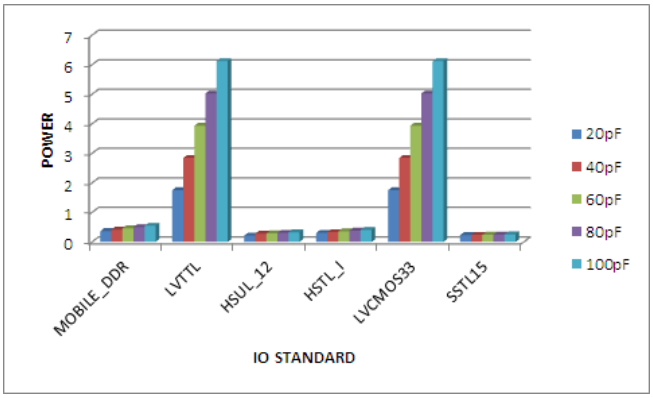

Figure 9. Power Dissipation at 25°Celsius Temperature for 2100 MHz

Table 7. Power Analysis at 50°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.417	0.461	0.506	0.550	0.594
LVTTL	1.806	2.902	3.999	5.096	6.195
HSUL_12	0.305	0.322	0.339	0.355	0.372
HSTL_I	0.355	0.380	0.404	0.429	0.453
LVCMOS33	1.806	2.902	3.999	5.096	6.195
SSTL15	0.277	0.283	0.289	0.295	0.301

There is 29.79% reduction in total power dissipation with MOBILE_DDR , 70.84% with LVTTL, 18.01% with HSUL_12, 21.63% with HSTL_I , 70.84% with LVCMOS33 , 7.97% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 7 and Figure 10.

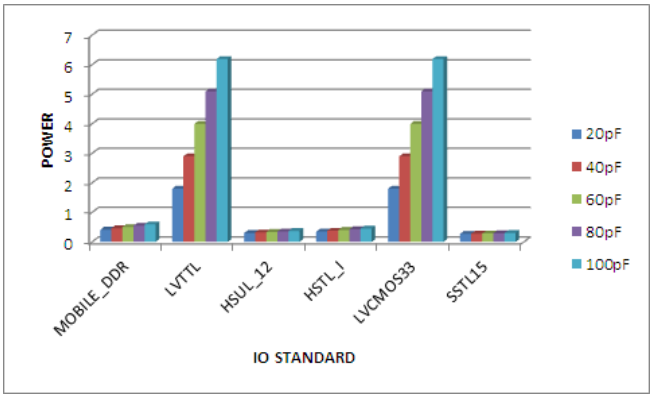

Figure 10. Power Dissipation at 50°Celsius Temperature for 2100 MHz

D. IO Power Analysis for 1700 MHz Frequency

Table 8. Power Analysis at 25°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.271	0.301	0.330	0.359	0.388
LVTTL	1.182	1.904	2.626	3.348	4.071
HSUL_12	0.202	0.213	0.225	0.236	0.247
HSTL_I	0.238	0.254	0.270	0.286	0.303
LVCMOS33	1.182	1.904	2.626	3.348	4.071
SSTL15	0.184	0.189	0.193	0.197	0.201

There is 30.15% reduction in total power dissipation with MOBILE_DDR , 70.96% with LVTTL, 18.21% with HSUL_12, 21.45% with HSTL_I , 70.96% with LVCMOS33 , 8.45% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 8 and Figure 11.

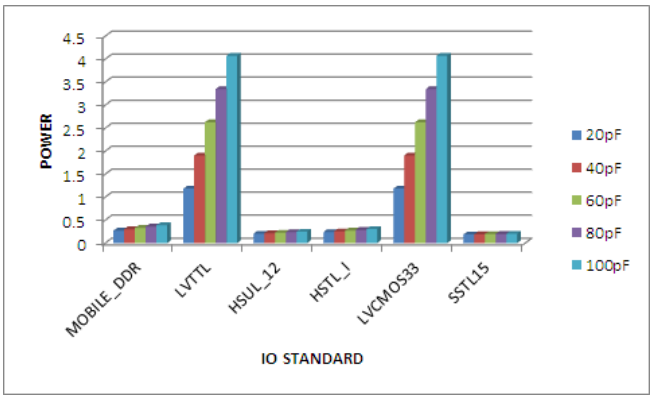

Figure 11. Power Dissipation at 25°Celsius Temperature for 1700 MHz

Table 9. Power Analysis at 50°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.315	0.345	0.374	0.403	0.433
LVTTL	1.229	1.954	2.680	3.406	4.132
HSUL_12	0.246	0.257	0.268	0.280	0.291
HSTL_I	0.281	0.298	0.314	0.330	0.347
LVCMOS33	1.229	1.954	2.680	3.406	4.132
SSTL15	0.228	0.232	0.236	0.240	0.244

There is 27.25% reduction in total power dissipation with MOBILE_DDR , 70.25% with LVTTL, 15.46% with HSUL_12, 19.02% with HSTL_I , 70.25% with LVCMOS33 , 6.55% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 9 and Figure 12.

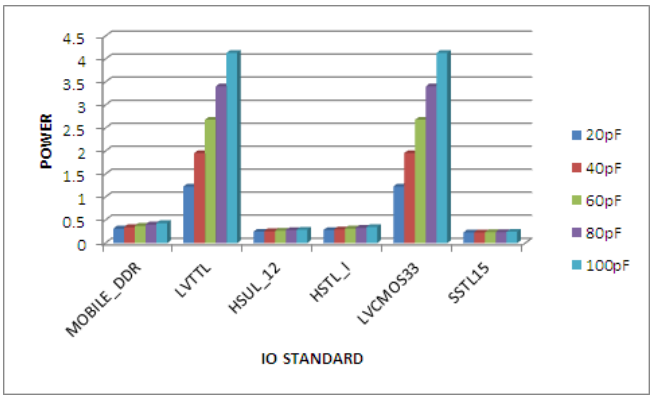

Figure 12. Power Dissipation at 50°Celsius Temperature for 2100 MHz

E. Power Analysis for 1800 MHz Frequency

Table 10. Power Analysis at 25°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.295	0.327	0.360	0.393	0.426
LVTTL	1.314	2.122	2.929	3.736	4.544
HSUL_12	0.216	0.228	0.241	0.253	0.266

HSTL_I	0.255	0.273	0.291	0.309	0.327
LVCMOS33	1.314	2.122	2.929	3.736	4.544
SSTL15	0.196	0.200	0.205	0.209	0.214

There is 28.02% reduction in total power dissipation with MOBILE_DDR , 70.52% with LVTTL, 15.30% with HSUL_12, 18.64% with HSTL_I , 70.52% with LVCMOS33 , 6.66% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 10 and Figure 13.

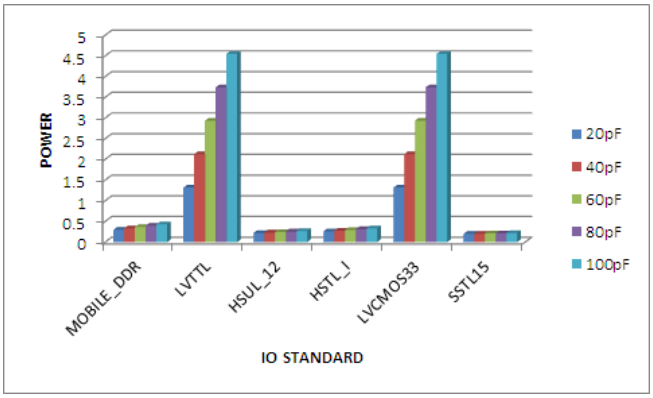

Figure 13. Power Dissipation at 25°Celsius Temperature for 1800 MHz

Table 11. Power Analysis at 50°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.339	0.372	0.404	0.437	0.470
LVTTL	1.362	2.173	2.984	3.796	4.607
HSUL_12	0.206	0.272	0.285	0.297	0.310
HSTL_I	0.298	0.317	0.335	0.353	0.371
LVCMOS33	1.362	2.173	2.984	3.796	4.607
SSTL15	0.239	0.244	0.249	0.253	0.258

There is 28.02% reduction in total power dissipation with MOBILE_DDR , 70.52% with LVTTL, 15.30% with HSUL_12, 18.64% with HSTL_I , 70.52% with LVCMOS33 , 6.66% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 11 and Figure 14.

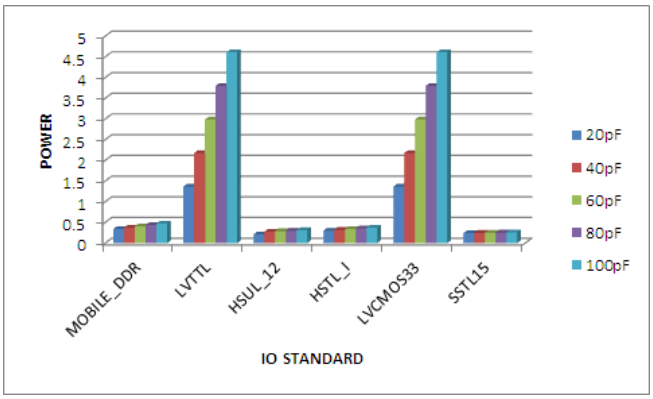

Figure 14. Power Dissipation at 50°Celsius Temperature for 1800 MHz

E. Power Analysis for 2.2 GHz Frequency

Table 12. Power Analysis at 25°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.401	0.449	0.498	0.546	0.595
LVTTL	1.918	3.113	4.309	5.505	6.701
HSUL_12	0.277	0.296	0.314	0.332	0.351
HSTL_I	0.331	0.358	0.385	0.412	0.439
LVCMOS33	1.918	3.113	4.309	5.505	6.701
SSTL15	0.247	0.253	0.260	0.267	0.273

There is 28.02% reduction in total power dissipation with MOBILE_DDR , 70.52% with LVTTL, 15.30% with HSUL_12, 18.64% with HSTL_I , 70.52% with LVCMOS33 , 6.66% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 12 and Figure 15.

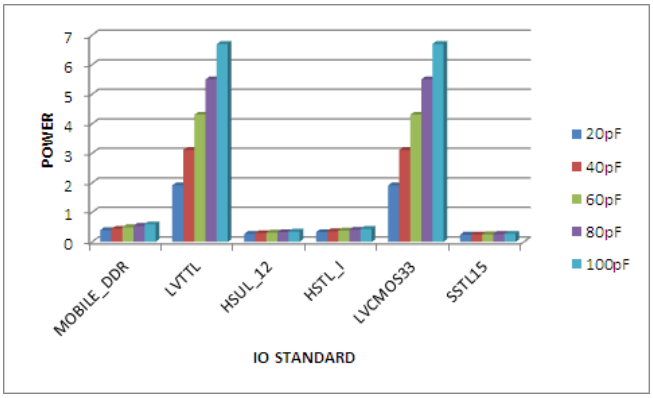

Figure 15. Power Dissipation at 25°Celsius Temperature for 2.2 GHz

Table 13. Power Analysis at 50°Celsius

IO STANDARD	20pF	40pF	60pF	80pF	100pF
MOBILE_DDR	0.445	0.494	0.543	0.591	0.640
LVTTL	1.969	3.170	4.371	5.574	6.777
HSUL_12	0.321	0.340	0.358	0.377	0.395
HSTL_I	0.376	0.402	0.429	0.456	0.483
LVCMOS33	1.969	3.170	4.371	5.574	6.777
SSTL15	0.290	0.297	0.304	0.311	0.317

There is 30.46% reduction in total power dissipation with MOBILE_DDR , 70.94% with LVTTL, 18.73% with HSUL_12, 22.15% with HSTL_I , 70.94% with LVCMOS33 , 8.51% with SSTL15 when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 13 and Figure 16.

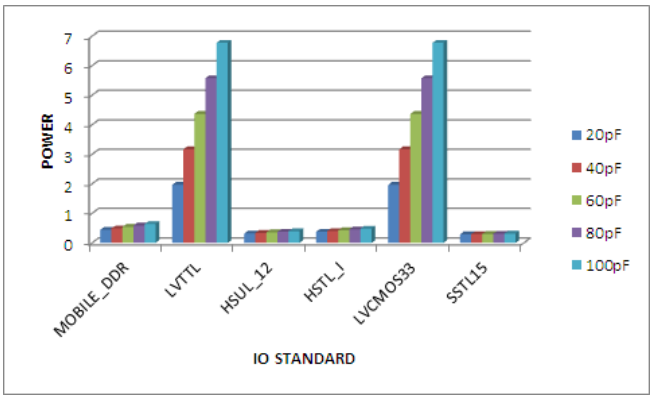

Figure 16. Power Dissipation at 50°Celsius Temperature for 2.2 GHz

F. Power Analysis for SSTL15 at different Capacitance and at different Frequencies

Table 14. Power Analysis at 25°Celsius

Frequency	20 pF	40 pF	60 pF	80 pF	100 pF
1400MHz	0.154	0.157	0.159	0.162	0.165
1.2GHz	0.136	0.138	0.140	0.142	0.145
2100MHz	0.233	0.239	0.245	0.251	0.258
1700MHz	0.184	0.189	0.193	0.197	0.201
1800MHz	0.196	0.200	0.205	0.209	0.214
2.2GHz	0.247	0.253	0.260	0.267	0.273

Table 14 and Figure 17 tells us that the maximum power is consumed at 2.2GHz and minimum power is consumed at 1.2GHz. In respect of capacitance maximum power is consumed at 100pF and minimum power is consumed at 20pF.

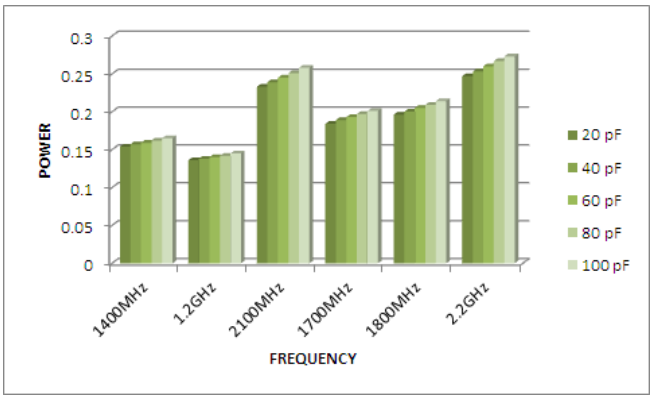

Figure 17. Power Dissipation at 25°Celsius Temperature for SSTL15 at Different Frequencies

Table 15. Power Analysis at 50°Celsius

Frequency	20 pF	40 pF	60 pF	80 pF	100 pF
1400MHz	0.197	0.200	0.203	0.206	0.209
1.2GHz	0.180	0.182	0.184	0.186	0.188

2100MHz	0.277	0.283	0.289	0.295	0.301
1700MHz	0.228	0.232	0.236	0.240	0.244
1800MHz	0.239	0.244	0.249	0.253	0.258
2.2GHz	0.290	0.297	0.304	0.311	0.317

Table 15 and Figure 18 tells us that the maximum power is consumed at 2.2GHz and minimum power is consumed at 1.2GHz. In respect of capacitance maximum power is consumed at 100pF and minimum power is consumed at 20pF.

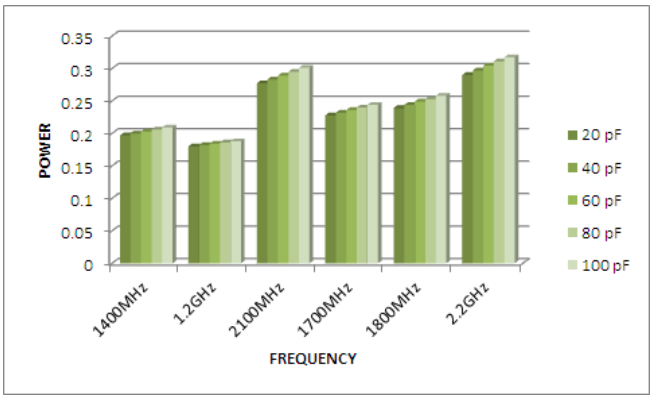

Figure 18. Power Dissipation at 50°Celsius Temperature for SSTL15 at different Frequencies

3. Conclusion

The design is energy efficient and the code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. . The wrist band will take the blood pressure as input and will tell about the state of the person wearing it. The design supports Internet of things service that's why IP addresses are involved. To design an energy efficient device we are using capacitance scaling and the capacitance is scaled down from 100pF to 20pF. During capacitance scaling, we observe that there is no change in clock power, logic power and signal power. Thermal Aware design is current research area. Analysis has been at two temperatures that is at 25 degree Celsius and at 50 degree Celsius. We can conclude from this design that the maximum power is consumed at 2.2GHz and minimum power is consumed at 1.2GHz. In respect of capacitance maximum power is consumed at 100pF and minimum power is consumed at 20pF for both 25degree Celsius and for 50 degree Celsius.

4. Future Scope

The future scope of "Capacitance Scaling With Different IO Standard Energy Efficient Wrist Watch on 28nm FGPA" is that we have used 28nm FGPA that is Kintex-7. We can also implement this design on 22nm or 18 nm FGPA. We can also use different FGPA families like automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive Spartan 3E, automotive Spartan6, Spartan3, Spartan3E. Here, we are using capacitance scaling techniques. We can redesign this design with other energy efficient technique like frequency scaling, thermal scaling, clock gating, and impedance matching with different logic family, and mapping. We can also change values of frequencies and can change the range of capacitance.

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