International Journal of Bio-Science and Bio-Technology
Vol.7, No.1 (2015), pp.71-80
http://dx.doi.org/10.14257/ijbsbt.2015.7.1.08

16-Channel Low Power CMOS Integrated Circuit for Detection of Auditory Nerve Signals

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Abstract

For sensorineural hearing loss, auditory perception can be activated by electrical stimulation of a nervous system via electrode implanted into cochlea or auditory nerves. As the tonotopic map of the human auditory nerve has not been absolutely identified, the recording of its signal with electrode is desirable to determine the map. This paper proposes a 16-channel analog front-end for auditory nerve signal detection. Its channel consists of an AC coupling circuit, a 4th-order Gm-C lowpass filter (LPF), and a single-slope analog-to-digital converter (ADC). While blocking DC level, the AC coupling circuit transfers only AC signal. The Gm-C LPF is designed with operational transconductance amplifiers (OTAs) using floating-gate technique for small Gm. The channel-wise single-slope ADC is used because it has the small area and low power consumption. Experiment results show the prototype chip fabricated in 0.35-μm CMOS process has the bandwidth of 0.1 ~ 6.95 kHz with the gain of 19.9 dB, the effective resolution of 7.7 bits and the power consumption per a channel of 12 μW.

Keywords: *analog front-end, auditory nerve, electrode, floating-gate, Gm-C filter*

1. Introduction

Hearing impairments are divided into conductive hearing loss and sensorineural hearing loss. The solutions to sensorineural hearing loss become more important, whereas conductive hearing loss can be corrected by a surgical operation. Among many solutions, one way is to use the auditory prosthesis which can recover the hearing ability by substituting electrical circuits with electrodes for malfunctioned auditory pathways [1, 2]. However, since the tonotopic map of the human auditory nerve has not been absolutely identified, the recording of the auditory nerve signal with electrode is desirable to determine the tonotopic map [3-7].

This paper proposes the low power 16-channel analog front-end for auditory nerve signal recording. A channel of the proposed analog front-end consists of an AC coupling circuit, a low-power 4th-order Gm-C lowpass filter (LPF), and a single-slope analog-to-digital converter (ADC). The LPF is implemented with operational transconductance amplifiers (OTAs) using floating gate technique [8] and a gain amplifier with the gain of 10 is embedded in the LPF to reduce the power consumption. Also, the readout speed is improved by adopting channel-parallel ADC structure, when compared with a conventional single ADC structure.

The rest of the paper is organized as follows. Next, the architecture of the proposed analog front- end is described. Section 3 provides the detailed circuit design. Section 4

ISSN: 2233-7849 IJBSBT

shows the experimental results of the fabricated chip. Finally, conclusions are provided in Section 5.

2. Structure of the Proposed Analog Front-End

Figure 1 shows the architecture of the proposed analog front-end to detect auditory nerve signal. The analog front-end detects nerve signal from auditory nerve by using an array of 16-channel electrodes. The AC coupling circuit, which consists of a capacitor and a PMOS transistor, transfers nerve signal without the effect of the uncertain DC voltage level. The proposed Gm-C LPF is designed with the cutoff frequency of 7 kHz and the gain amplifier with the gain of 20 dB is embedded in the LPF to reduce power consumption, when compared with the case that the amplifier is designed separately. After 16-channel nerve signals are filtered, they are simultaneously digitized by the 16-channel ADCs. A channel-parallel ADC is designed as the structure of a single-slope ADC which occupies the small silicon area, because the ADC needs the sampling rate of 40 kS/s and the resolution of 8 bit to detect auditory nerve signal. Also, the digitized data are readout by a serializer to reduce the number of the output interface lines.

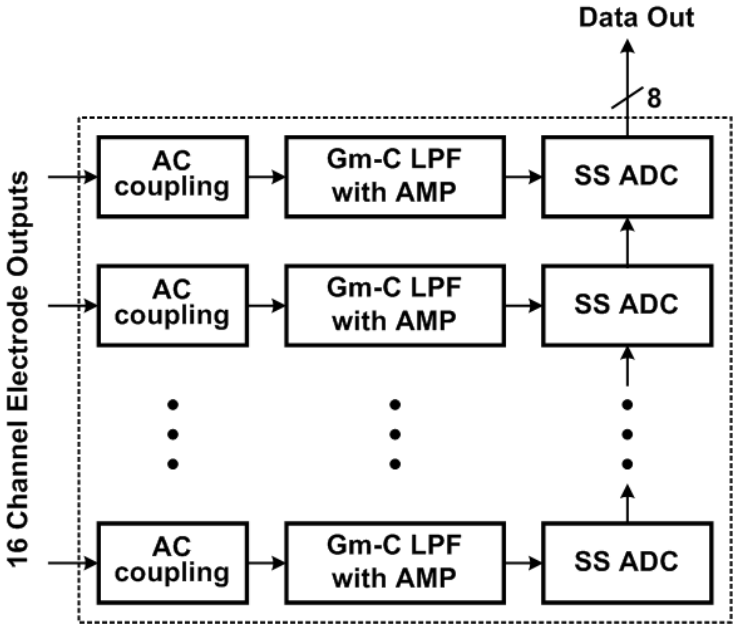

Figure 1. Block Diagram of the Proposed 16-channel Analog front-end for Auditory Nerve Signal Detection

3. Circuit Implementation of the Proposed Analog Front-End

3.1. AC Coupling Circuit

Figure 2 shows the AC coupling circuit that transfers only AC signal, while blocking DC level. Since auditory nerve signal detected by the electrode is in a floating state, the AC coupling circuit is needed to provide the proper input common-mode voltage for the operation of the LPF. Although the conventional AC coupling circuit is implemented with the combination of the external large capacitor and resistor, the proposed AC

coupling circuit is implemented with the small capacitor C_{ac} and the large channel resistance of the transistor M_{ac} controlled by the bias voltage V_b, because the proposed analog front-end is an integrated chip (IC) and its silicon area is reduced.

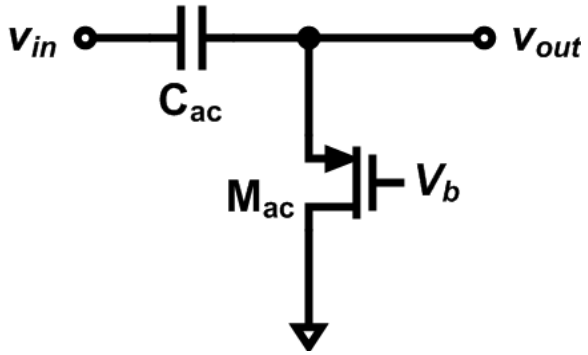

Figure 2. AC Coupling Circuit

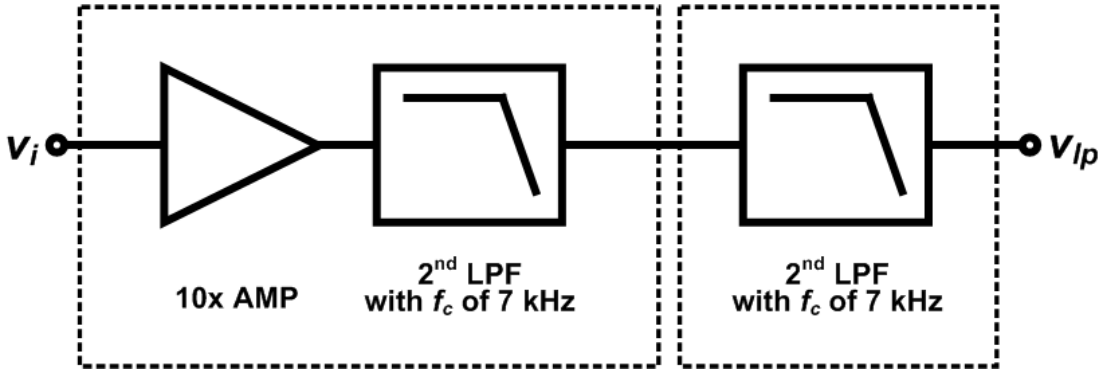

Figure 3. Block Diagram of the Proposed 4th-order Gm-C LPF with a 10x Amplifier

3.2. Gm-C LPF

Figure 3 shows the block diagram of the proposed 4th-order LPF. The proposed 4th-order LPF has the cascade structure that successively consists of two 2nd-order Gm-C LPFs. Also, the 2nd-order LPF at the first stage embeds the amplifier with the gain of 20 dB to amplify auditory nerve signal which has the small signal range and reduce power consumption and silicon area, when compared with the case that the amplifier is designed separately.

Figure 4 shows the schematic diagram and the signal flow graph of the 2nd-order Gm-C LPF that is the functional block of the proposed 4th-order Gm-C LPF. The 2nd-order Gm-C LPF is implemented with three OTAs with three transconductances g_{m1}, g_{m2}, and g_{m3}. If $g_{m2} = g_{m3} = g_m$ and $C_1 = C_2 = C$, the transfer function of the 2nd-order LPF can be obtained as Equation (1) from the signal flow graph.

$$\frac{V_{LP}(s)}{V_I(s)} = \frac{\frac{g_{m1} g_m}{C^2}}{s^2 + \frac{2 g_m}{C} s + \frac{g_m^2}{C^2}} \qquad (1)$$

Here, the voltage gain of the 2nd-order LPF, A_v is obtained as g_{m1}/g_m V/V and the cutoff frequency f_c is obtained as $g_m/2\pi C$ Hz.

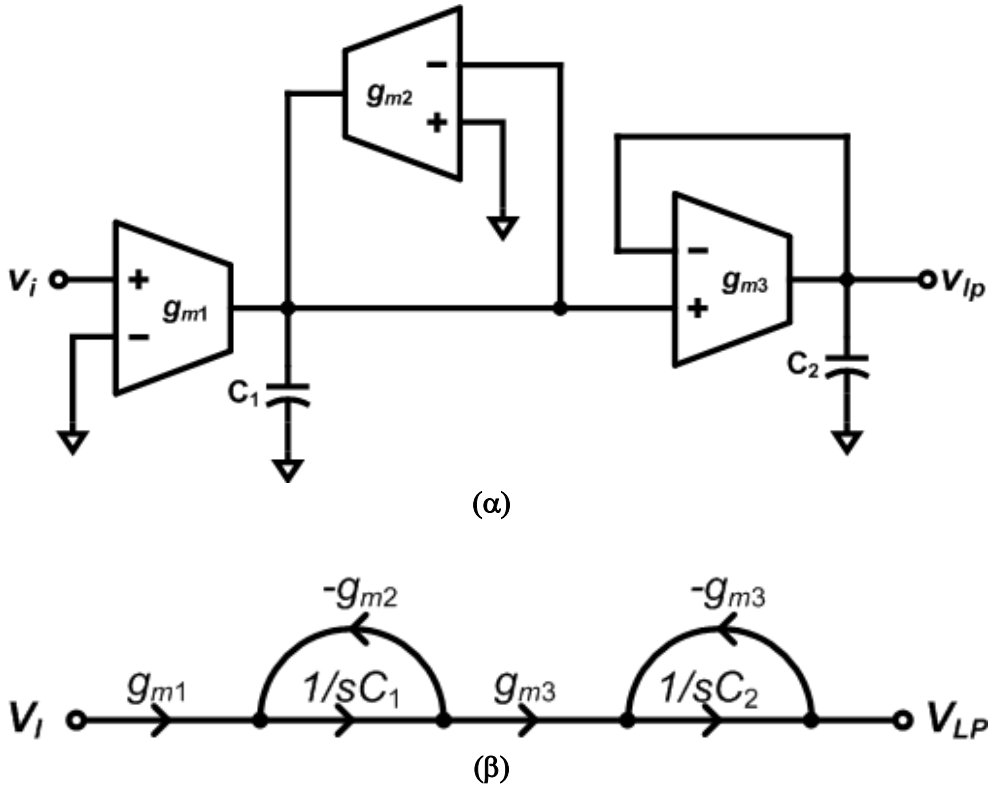

Figure 4. (a) Schematic Diagram and (b) Signal Flow Graph of the 2nd-order Gm-C LPF

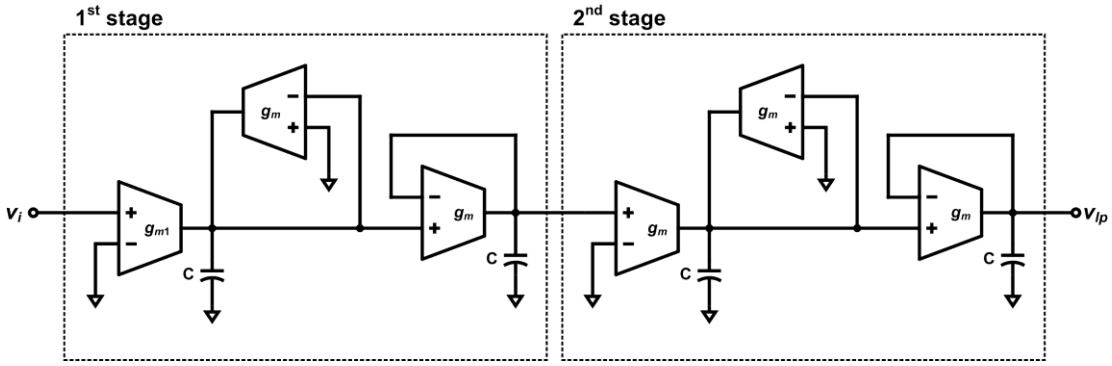

Figure 5. Schematic Diagram of the 4th-order Gm-C LPF

Figure 5 shows the total schematic diagram of the 4th-order Gm-C LPF used in this paper. The 4th-order Gm-C LPF is implemented as the cascade structure that successively consists of two 2nd-order Gm-C LPFs and has the voltage gain of 20 dB that is adjusted by the ratio of g_{m1} and g_m in the 2nd-order LPF at the first stage. The 2nd-order LPF at the second stage has the voltage gain of 0 dB, because all OTAs have the same transconductance. Table 1 shows

the parameters of the 4th-order Gm-C LPF to achieve the voltage gain of 20 dB and the cutoff frequency of 7 kHz.

Table 1. Parameters of the 4th-order Gm-C LPF

Transconductance	g_{m1}	682 nA/V
	g_m	68.1 nA/V
Capacitance	C	1.55 pF

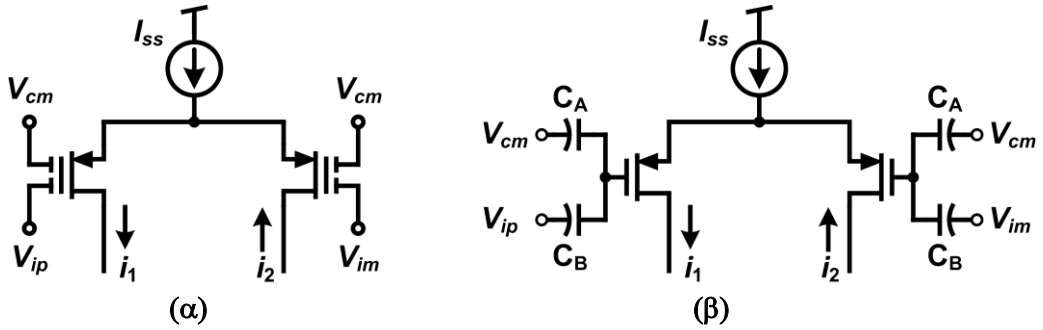

Figure 6. Transconductance Reduction Technique with Floating Gate

Figure 6 shows the transconductance reduction technique with floating gate. The floating gate technique is used in the input stage of the conventional OTA to achieve smaller transconductance than that of the conventional OTA. Instead of using double poly CMOS process as shown in Figure 6 (a), the same result can be obtained by using two capacitors implemented from the normal CMOS process as shown in Figure 6 (b). The effective transconductance, G_m of the proposed OTA is decreased as Equation (2) by the floating gate technique.

$$G_m = \frac{C_A}{C_A + C_B} g_m \qquad (2)$$

where g_m is the transconductance of the input transistor. Figure 7 shows the schematic of the OTA using floating gate technique.

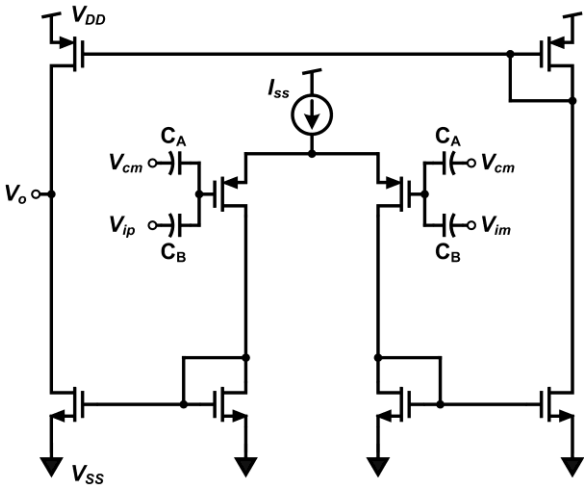

Figure 7. Schematic of the OTA using Floating Gate Technique

3.3. Single-Slope ADC

Figure 8 shows the block diagram of the channel-parallel single-slope ADC. The output of the LPF is sampled/held by the switch and the capacitor C_{sh}. Then the 8-bit counter starts and the ramp signal ramps concurrently. When the ramp signal exceeds the voltage sampled in C_{sh}, the output of the comparator changes from 'Low' state to 'High' state. At this moment, the register latches the counter value [9]. This counter value is the digitized data of the LPF output.

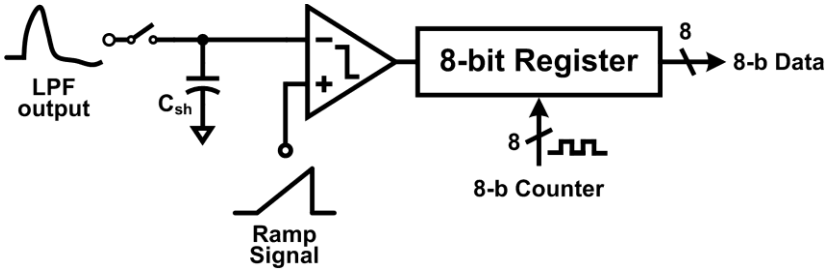

Figure 8. Block Diagram of the channel-parallel single-slope ADC

4. Experimental Results

The layout of the fabricated chip is shown in Figure 9. The chip is fabricated with 0.35-μm 1-poly 4-metal CMOS process and the core area is 2.6 mm x 3.7 mm and operates at power supply of 3.0 V. The AC coupling circuit and the Gm-C LPF have the input common-mode voltage of 1.5 V. The input ranges of the Gm-C LPF and the single-slope ADC are 100 mV and 1 V respectively. The ADC has the sampling rate of 40 kS/s.

Figure 10 shows the photograph of the test PCB board for the prototype chip. The power supply, current, reference voltage, and control signal are provided into the inside of the chip from mother board through the flexible cable. Also, the digitized output can be transferred through the flexible cable.

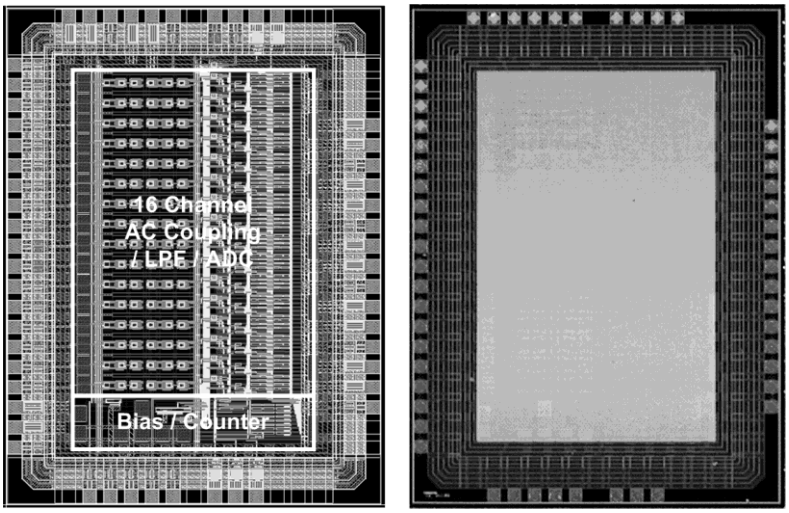

Figure 9. Layout and Microphotograph of the Prototype Chip for the Proposed Analog Front-End

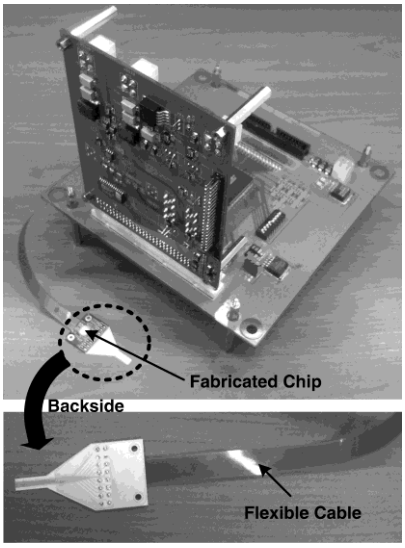

Figure 10. Photograph of the Test Board for the Prototype Chip

Figure 11 shows the comparison between the simulation result and the experimental result of the frequency response for the sinusoidal input signal with the magnitude of 80 mV. It is observed that the signal under the frequency of 100 Hz is attenuated, the cutoff frequency is about 6.95 kHz, and the passband gain is about 19.9 dB as expected by the simulation.

Figure 12 shows the measured output spectrum of the single-slope ADC for -8 dB_{FS}, 1 kHz sinusoidal input. The measured signal to noise-plus-distortion ratio (SNDR) and effective resolution are 48 dB and 7.7 bits respectively.

The power consumption per a channel is measured as 12 μW. Table 2 shows the performance summary.

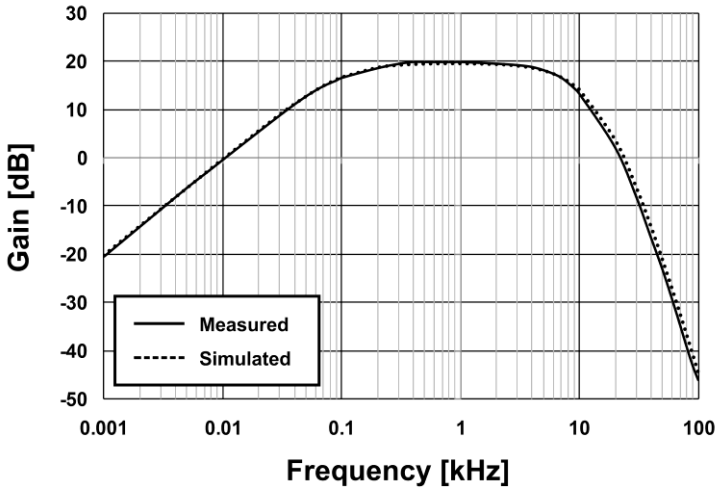

Figure 11. Frequency Response for the Sinusoidal Input Signal with the Magnitude of 80 mV

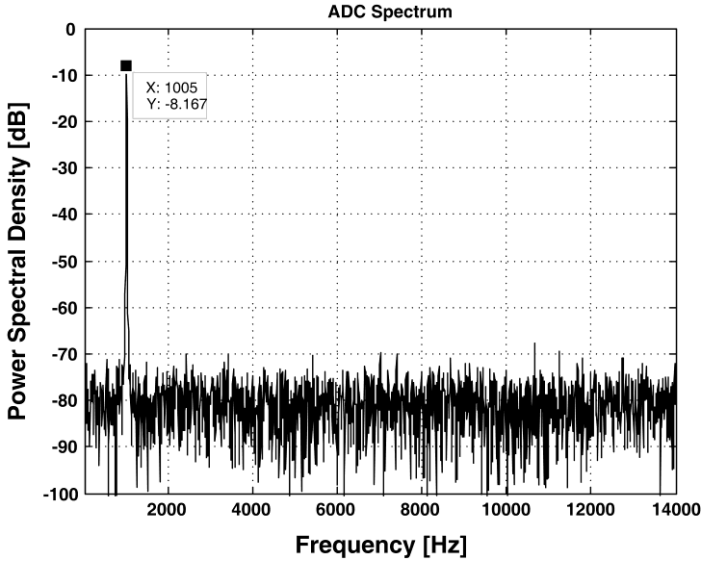

Figure 12. Measured Output Spectrum of ADC for -8 dB_{FS}, 1 kHz sinusoidal input

Table 2. Performance Summary

Technology	0.35-μm 1P4M
Supply voltage	3.0 V
Gm-C LPF cutoff frequency	6.95 kHz

Gm-C LPF gain	19.9 dB
ADC sampling rate	40 kS/s
Effective resolution	7.7 bits
ADC INL/DNL	< ±0.5 LSB
Power consumption per a channel	12 μW

5. Conclusions

We proposed the 16-channel analog front-end for auditory nerve signal detection. A channel of the proposed analog front-end consists of an AC coupling circuit, a low-power 4th-order Gm-C LPF, and a single-slope ADC. The AC coupling circuit transfers only AC signal while it blocks DC signal level. Considering the bandwidth of the auditory signal, the Gm-C LPF is designed with OTAs adopting floating-gate technique. For the channel-parallel ADC structure, the single-slope ADC is used because it occupies the small silicon area. Experimental results shows that the AC coupling circuit and LPF have the bandwidth of 100 Hz ~ 6.95 kHz and the ADC has the effective resolution of 7.7 bits. The power consumption per a channel is 12 μW, the power supply is 3.0 V, and the core area is 2.6 mm × 3.7 mm. The proposed analog front-end was fabricated in a 1-poly 4-metal 0.35-μm CMOS process.

Acknowledgements

This paper was supported by Research Fund, Kumoh National Institute of Technology.

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Jimin Cheon, he received the B.S., M.S., and Ph.D degrees in electrical and electronic engineering from Yonsei University, Seoul, Korea in 2003, 2005 and 2010, respectively. From 2010 to 2012, he was a senior engineer with the Image Development Team of System LSI Division at Samsung Electronics in Yongin, Korea working on the design of APS-C CMOS image sensors for mirrorless and DSLR cameras. From 2012 to 2013, he was a manager with the Semiconductor Tech. Laboratory of Fusion Technology R&D Center at SK telecom in Seongnam, Korea working on the design of automotive CMOS image sensors with SK hynix. In 2013, he joined Kumoh National Institute of Technology as an Assistant Professor in the school of electronic engineering, working on the design of CMOS image sensors, low-power data converters, high performance sensors and interface circuits.