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An Implementation of Parasitic Insensitive 128 x100 Pixels Fingerprint Sensor using Modified Switched Capacitor Integrator

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Abstract

This paper proposes 128x100 array fingerprint sensor with the modified parasitic insensitive switched capacitor integrator. The modified parasitic insensitive switched capacitor integrator includes four switches to eliminate parasitic capacitance and transfer a generated charge. The proposed circuit also frees from the influence of skin resistivity, because the effect of the voltage drop through skin resistor is very small. The scheme of one pixel includes a pixel level charge transfer and also parasitic insensitive switched capacitor integrator with a differential amplifier. The proper operation is validated by HSPICE for one-pixel and RTL simulation including logic synthesis for a full chip design on condition of 0.35μm typical CMOS process and 3.3V power. The layout is performed by full custom flow for one-pixel and auto P&R for a full chip. The area of a full chip is 8721 μm x 6921 μm and the gate count is 1,140,553. The area of one-pixel is 58 x 58 μm^2. Pitch is 60 μm and image resolution is 423dpi.

Keywords: *Switched Capacitor Integrator, Parasitic Insensitive, Charge Transfer, Fingerprint Sensor, RTL synthesis, HDL*

1. Introduction

Small-size capacitive fingerprint sensors using the CMOS process have been developed for low power, low cost [1-3]. Recently, the solid-state capacitive fingerprint sensors are adopted on mobile application environment like a smartphone. Most of them rely on capacitive coupling between the finger and matrix of small metal plates to detect ridges and valleys on the finger surface. Each plate forms a pixel of the resulting image and requires circuitry to measure the capacitance using. One of the most important performances of a capacitive sensor is the sensitivity capability since the detected capacitance is very small of the order of femto-farads. Figure 1 shows a typical charge-sharing sensing scheme with a parasitic capacitance insensitive circuit and sensing signal amplifier using a unit-gain buffer[4-6]. The series-connected capacitor Cf is composed of a capacitor between the metal plate and the chip surface and another one between the chip surface and the finger skin. The capacitance of Cf is at its maximum value when a ridge has contact with the passivation layer. In figure 1, "SA" is a unit-gain buffer. At the beginning of the unit-gain phase, the charges stored in the precharge are redistributed between the nodes. The SA tracks the voltage change of the node Vsa, which makes the potential difference between the two electrodes of Cp3 zero. In the sensing phase, SA operates as an attenuator by R1 and R2 ratio. The voltage difference between the contacted point (ridge) and the non-contacted point (valley) was about vdd/2 on 0.35μm typical process parameter and 3.3V power supply. Therefore, the circuit can be estimated as a parasitic capacitance insensitive scheme. Even though the typical charge sharing circuit is parasitic insensitive and detects wide sensing voltage range, there are some disadvantages like using process dependent resistors with static current and the complex vertical structure as shown in figure 2. The fingerprint sensor is fabricated in low cost using low level process like 0.35 μm or 0.18 μm in general, because the size of chip have to cover fully a finger skin area. In Figure 2, the circuit needs top metal and under metal for parasitic

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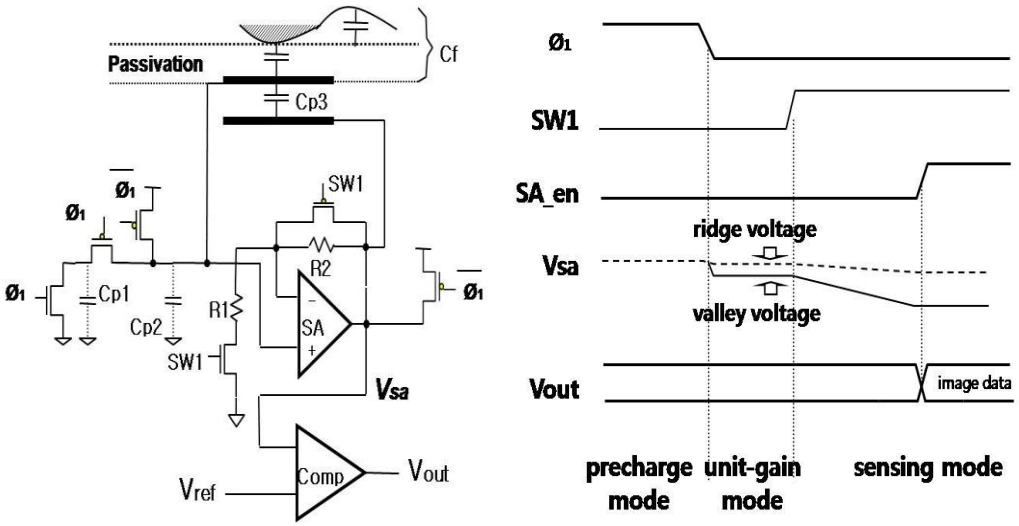
insensitive operation between input and output of unit-gain buffer. Metal 2 is shielding metal and therefore, there are only metal 1 and poly layer for routing nets. That means these circuits may show the weakness in SNR.

This paper proposes novel parasitic insensitive fingerprint sensor with the modified switched capacitor integrator [7-8]. The scheme of one pixel includes a pixel level charge transfer and parasitic insensitive switched capacitor integrator with a differential amplifier in Section 2.1 and 2.2. This paper proposes an area type 128x100 array fingerprint sensor LSI. The proper operation is validated by HSPICE for one-pixel and RTL simulation including logic synthesis for a full chip design on condition of 0.35μm typical CMOS process and 3.3V power. The layout is performed by full custom flow for one-pixel and auto P&R for a full chip. The concept and design result of the proposed sensing scheme is described in Section 2.3.



(a) Sensing Circuit (b) Timing Diagram

Figure 1. Typical Parasitic Insensitive Capacitive Fingerprint Sensing Scheme

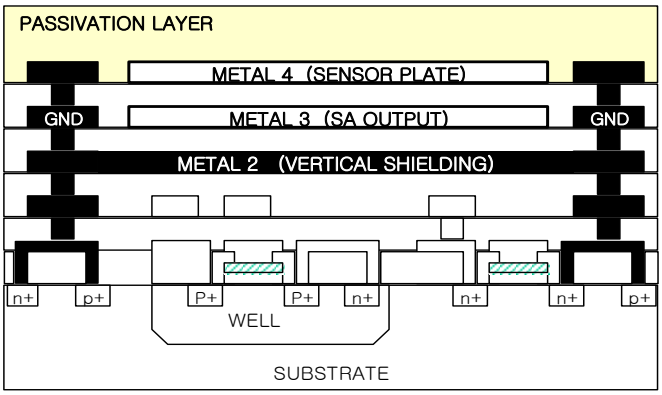


Figure 2. Horizontal and Vertical Isolation Structure of Typical Sensor

2. Proposed Sensing Scheme

2.1. Charge Transfer Switched Capacitor Integrator without a Parasitic Capacitance

This section introduces a parasitic insensitive charge transfer circuit and analyzes its charge transfer operation which is modified with a parasitic-insensitive switched capacitor integrator [7]. Capacitive sensing devices may suffer from more parasitic

components in their touch sensitivity and performance. To eliminate this parasitic influence, a parasitic insensitive switched capacitor integrator can be used [8]. Figure 3 shows a parasitic-insensitive switched capacitor integrator as a capacitive touch sensing circuit and timing diagram. The clock signals, Φ 1, Φ 2, control switches and the resulting output voltage of the integrators are shown in Figure 3. When Φ 1 is on, the node of the parasitic capacitor, Cp2, is charged to VDD/2. The node of negative input of an opamp is virtually shorted to the positive input whose potential is VDD/2 in the circuit. Therefore, there are no charges transferred from Cp2 to Cs because the two nodes of Cp2 are of the same potential with that of the output node whose charges are transferred from Ct to Cs. Therefore, the overall transfer function of the proposed circuit does not include parasitic capacitance as represented in equation 1, where z is a parameter from z-transform. When Φ 2 is on, the node of the parasitic capacitor, Cp1, is charged to ground. So, the influence of all parasitic capacitance is removed. The capacitor Cs integrates transferred charge from the fingerprint capacitor Cf at Φ 2 rising time. Through the value of Cf, the slope of curve is different. The value of Cf is big value at a ridge and is small at a valley.

$$H(z) = \frac{C_f}{C_s} \cdot \frac{1}{z-1} \tag{1}$$

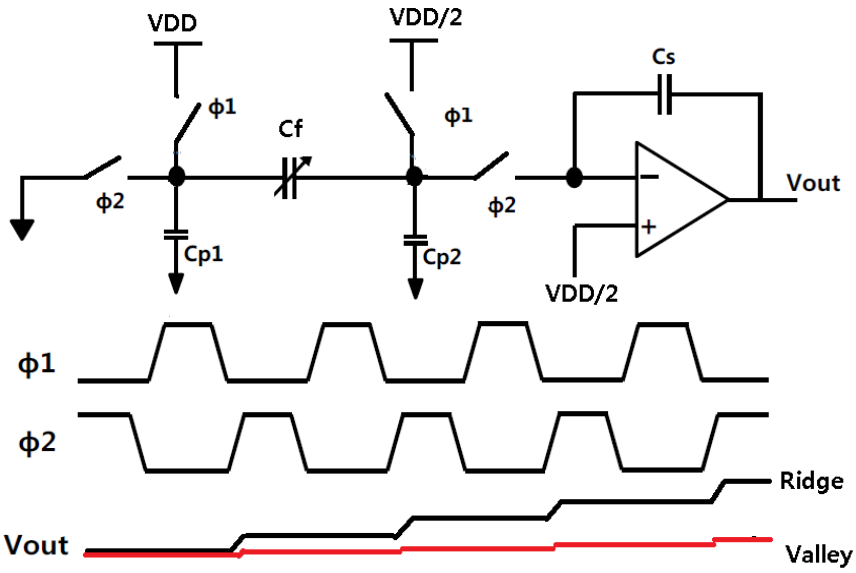


Figure 3. Charge Transfer Switched Capacitor Integrator Circuit

2.2. Design of Fingerprint Sensor with the Switched Capacitor Integrator

Figure 4 and 5 show the proposed fingerprint sensor one pixel with a parasitic-insensitive charge transfer switched capacitor integrator circuit. Finger skin is modeled with Cf and Rf. A variable capacitor, Cf, represents the capacitor formed between a fingerprint sensor top plate and skin. Rf represents a skin resistance. The parasitic capacitors Cp1, Cp2 are removed by controlling the switching signal “p1” or “p2”. To confirm this effect, we extracted each parasitic capacitance from the optimized layout of sensor one-pixel. Cp1 and Cp2 are 43fF and 80fF. The Cf of a ridge capacitance is the same as passivation capacitor (Cox = 42fF). The valley capacitance is less than 1fF. Feedback capacitor Cs is 500fF. An improvement can be seen by the HSPICE simulation of the cell with condition of 0.35μm typical parameter and 3.3V power supply after layout extraction. Figure 6 shows the timing operation at a ridge, valley and between a ridge and valley. The voltage difference between a contacted point

(ridge) and non-contacted point (valley) is about 1550mV after 10 clock cycles. That means the proposed scheme result is almost same with VDD/2 of full swing range as shown in figure 6. The maximum frequency of cell operation is 40MHz, when the output reaches from VDD/2 to VDD within 10 clocks. We simulate from Cp1 x1, Cp2 x1 to x10 for the variation effect of a parasitic capacitance, then the output voltage variation is less than 2%. The simulation results show the parasitic insensitive characteristics which increase touch sensitivity of the circuit.

In fingerprint sensing, the image quality degrades when the finger is dry. The reason for the degradation is explained using an equivalent circuit model of the finger with the sensing circuit as shown in Figure 4. The finger model is given by the series connection of the sensed capacitance and the resistance of the finger surface Rf. Skin resistivity varies from one person to another and depends also on skin humidity and mechanical pressure applied on the sensor. A skin resistivity varies from 1 MΩ to 10 MΩ in dry conditions. A resistivity of 100 KΩ has been measured in the case of humid skin[4]. The proposed circuit free from the influence of skin resistivity if there is no problem in time margin, because the effect of the voltage drop through skin resistor Rf is very small as shown in Figure 7.

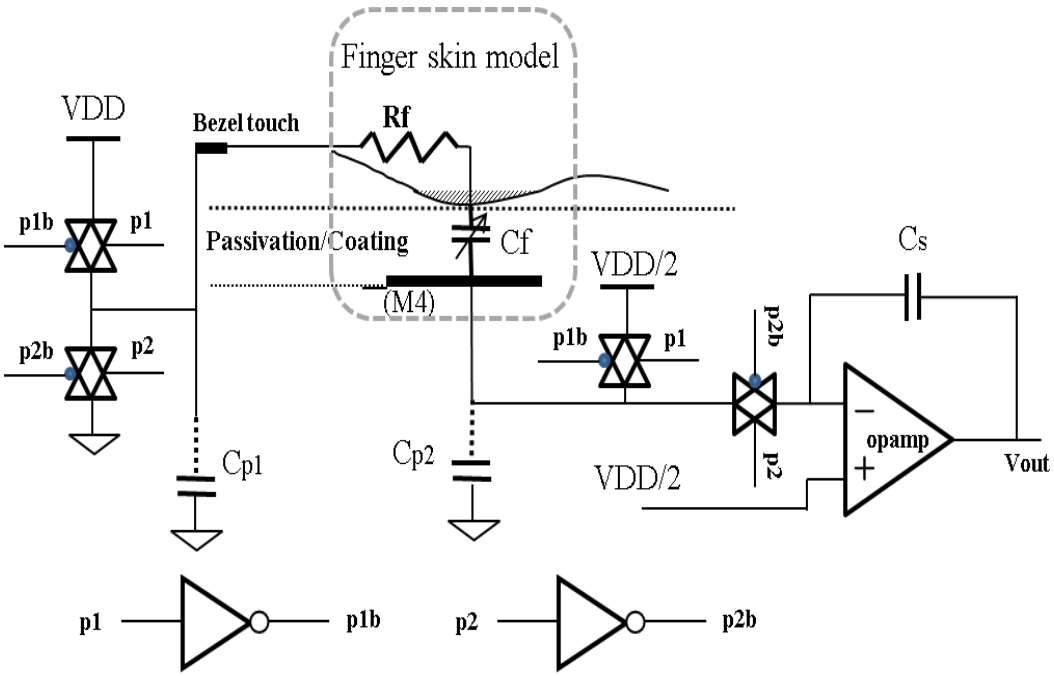


Figure 4. One Pixel Circuit of Proposed Sensor

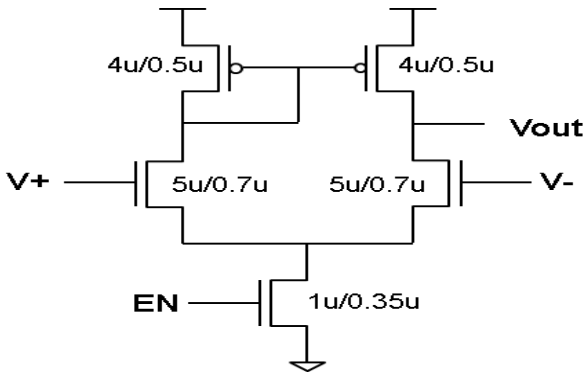


Figure 5. Simple Opamp for One Pixel Layout

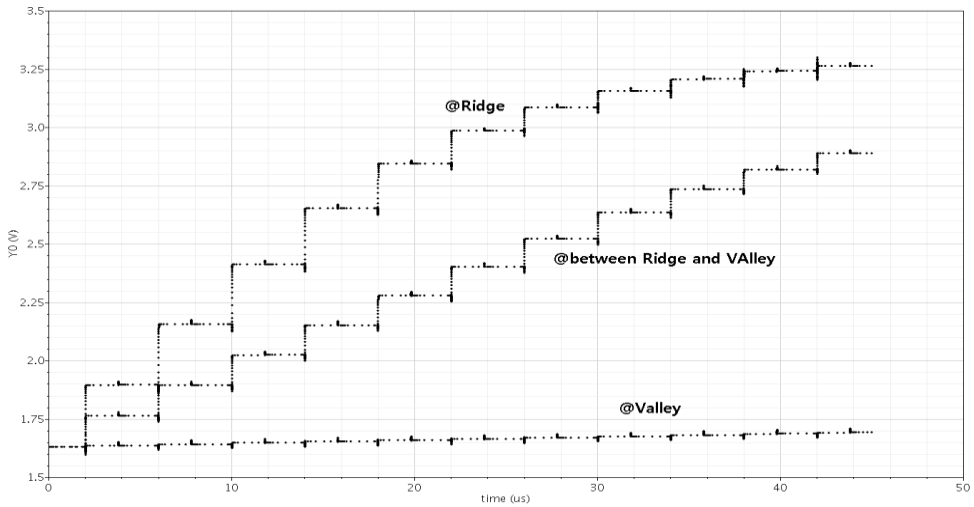


Figure 6. Time Domain Voltage Output Characteristics of Proposed Sensor Circuit (0.35μm Typical Parameter and 3.3V Power Supply)

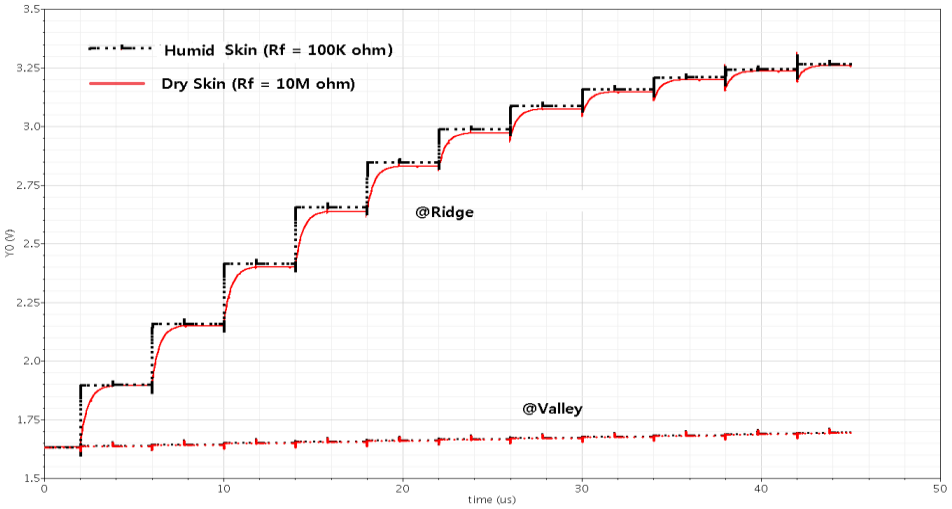


Figure 7. Output Characteristics on Dry and Humid Skin (0.35μm Typical Parameter and 3.3V Power Supply)

2.3. LSI Implementation of Proposed Sensing Technique

Figure 8 shows the chip block diagram of the proposed area type fingerprint sensor with 128x100 pixel. Figure 9 shows the design flow of chip implementation. Figure 10 shows 128x10 pixel array chip layout and the area is 8721μm x 6921μm on 0.35μm standard CMOS process. The layout area of one pixel is 58μm x 58μm and pixel pitch is 60μm. The gate count is 1,140,553. The layout of 128x100 array core cell is performed by full custom design method and the full chip is performed by auto placement and routing of cell based design method.

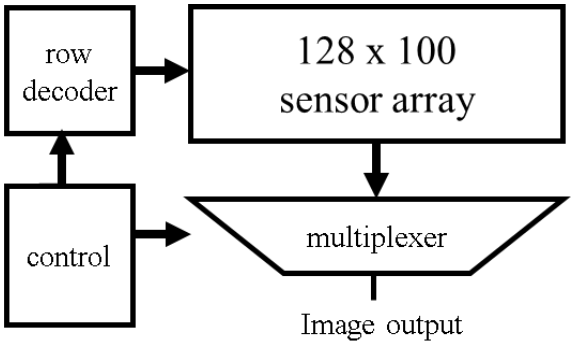


Figure 8. Chip Architecture

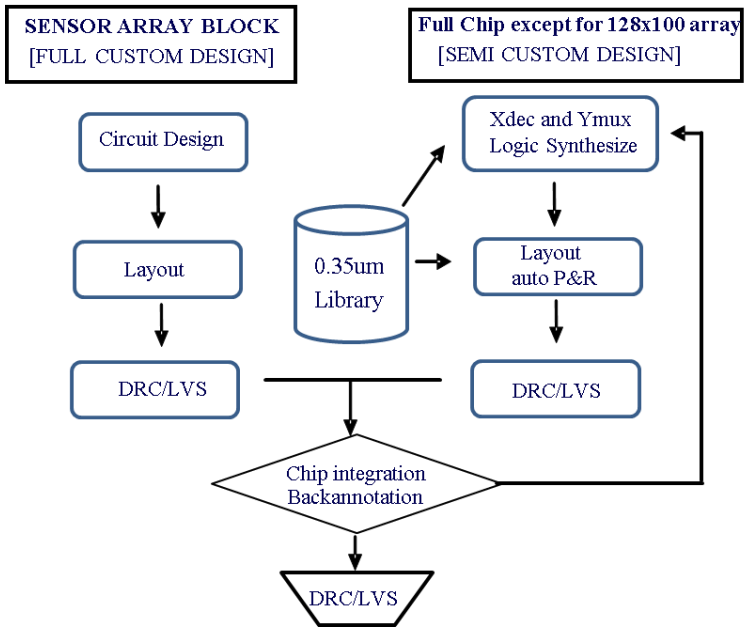


Figure 9. Design Flow of Fingerprint LSI

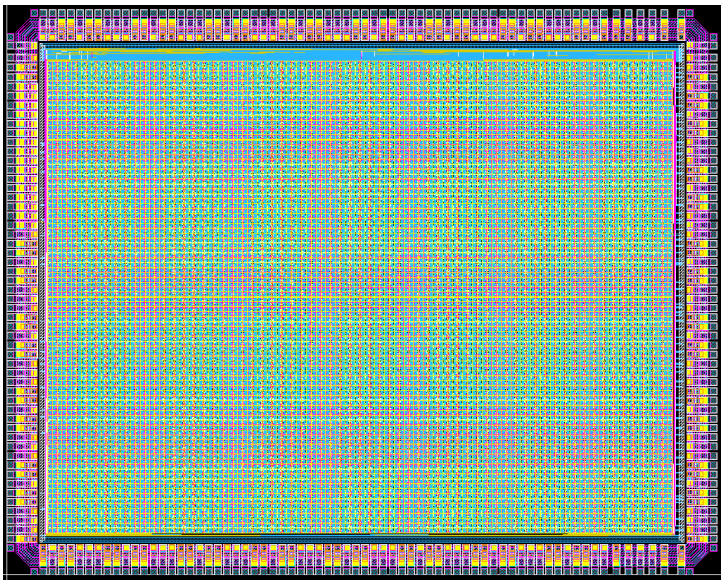


Figure 10. 128x100 Pixel Array Chip Layout (8721 μm x 6921 μm @0.35μm CMOS Process)

3. Conclusion

This paper proposes novel parasitic insensitive fingerprint sensor with the modified switched capacitor integrator. The scheme of one pixel includes a pixel level charge transfer and parasitic insensitive switched capacitor integrator with a differential amplifier. Even though the typical charge sharing circuit is parasitic insensitive and detects wide sensing voltage range, there are some disadvantages like using process dependent resistors with static current and the complex vertical structure. That means these circuits may show the weakness in SNR. The modified parasitic insensitive switched capacitor integrator includes four switches to eliminate parasitic capacitance and transfer a generated charge. An improvement can be seen by simulation of the cell with condition of 0.35μm typical parameter and 3.3V power supply after layout extraction. The voltage difference between the contacted point (ridge) and the non-contacted point (valley) is about 1550mV after 10 clock cycles. The maximum frequency of cell operation is 40MHz, when the output reaches from VDD/2 to VDD within 10 clocks. The output voltage variation by parasitic capacitance is less than 2%. The proposed circuit frees from the influence of skin resistivity if there is no problem in time margin, because the effect of the voltage drop through skin resistor is very small. The results show the parasitic insensitive characteristics which increase touch sensitivity of the circuit. The proper operation is validated by HSPICE for one-pixel and Verilog-HDL for a full chip simulation with condition of 0.35μm typical CMOS process and 3.3V power. Full chip logic is synthesized and integrated with 128x100 array sensor core. The layout is performed by full custom flow for one pixel and auto P&R for a full chip. The area of a full chip is 60.4 mm^2 (8721μm x 6921μm) with 244 input and output pads. The gate count is 1,140,553 and one-pixel is 58 x 58 μm^2 and image resolution is 423dpi.

Acknowledgement

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