Design of Low Power and High Speed CMOS Fingerprint Sensor

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Abstract

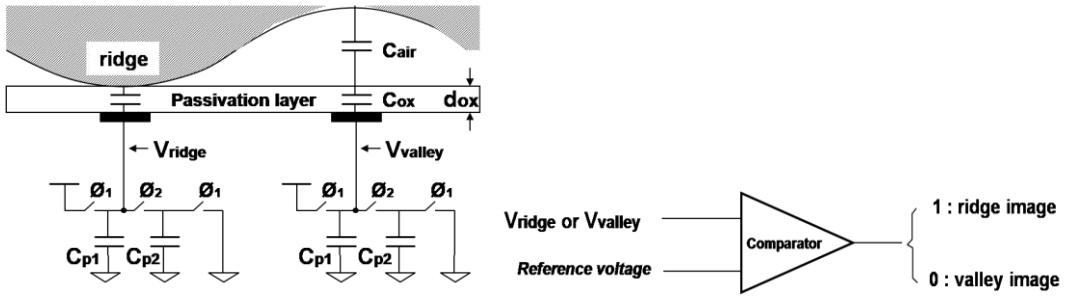
This paper proposes two topics for a high performance fingerprint sensor. A modified capacitive detection circuit of charge sharing scheme is proposed, which shows 40% reduction of power consumption and 90% improvement of difference between a ridge and valley sensing voltage than typical scheme. This paper also proposes an effective fingerprint identification system with hardware unit (thinning processor) for thinning stage processing of a verification algorithm based on minutiae. Each step of a fingerprint algorithm is analyzed on FPGA and ARMulator. The proposed scheme just needs 56,000 cycles for a thinning processing in 160x192 pixel array and the layout area is 0.541 mm^2 at 0.35μm CMOS process.

Keywords: *Biometrics, Fingerprint, Sensor, thinning, algorithm, VLSI*

1. Introduction

Traditional automatic personal identifications, such as personal identification numbers (PINs), identification cards, and keys are no longer satisfactory for recent security requirements. Biometrics, the automatic identification of a person on the basis of certain physiological or behavioral characteristics, is one of the technologies that can be applied to the fulfillment of security requirements, because each individual has unique characteristics that are relatively constant over time [1]. The fingerprint is known to be the most representative bio-metric for authentication of individual persons. Some research organizations have published papers on semiconductor-based sensing schemes and demonstrated the possibility of a single-chip solution.

A capacitive fingerprint sensor uses a capacitive sensor array to detect fingerprints. The name ‘capacitive’ comes from the fact that the finger skin and the sensor electrode produce a capacitor whose capacitance is determined by the distance from the chip surface to the finger skin. The finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode as shown in Figure 1. One of the most important performances of a capacitive sensor is the sensitivity capability since the detected capacitance is very small of the order of femto-farads. A charge-sharing sensing scheme has a high sensitivity and a simple circuit structure for the restricted pixel area below a sensor plate. Some papers on charge-sharing sensing scheme have been published [2, 3, 4]. The paper [2] proposed the removing of parasitic capacitance using unit-gain buffer, and paper [3, 4, 5, 6] proposed the improvement of difference between a ridge and valley detection voltage using a feedback resistor. Although these methods are useful in dramatic performance improvement, a static current can exist on a sensing enable phase in these circuits because of a unit-gain buffer and feedback resistor. This paper proposes a modified circuit for reduction of the static power dissipation.



(a)

(b)

Figure 1. Model of capacitive fingerprint sensing scheme: (a) charge sharing sensing scheme, (b) detection of a ridge and valley using comparator

A fingerprint verification algorithm has two phases: enrollment and verification. In the off-line enrollment phase, an enrolled fingerprint image is preprocessed, and the minutiae are extracted and stored. In the on-line verification phase, the similarity between the enrolled minutiae and the input minutiae is examined. There are three steps involved in the verification process: 1) image preprocessing, 2) minutiae extraction, and 3) minutiae matching [7]. Conventional fingerprint authentication hardware and software system needs a high performance microcontroller such as 32-bit ARM7, or ARM9. Figure 2 shows a conventional fingerprint system.

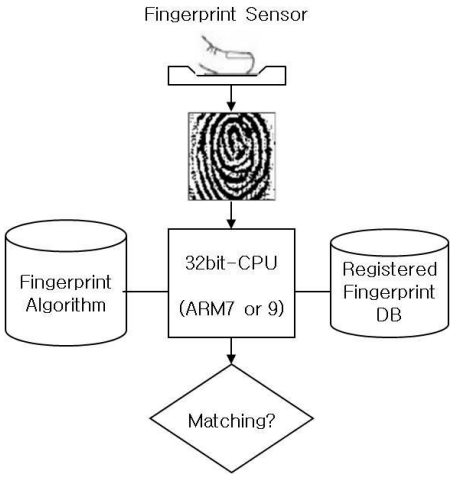


Figure 2. Typical fingerprint identification system

This paper proposes an effective hardware unit for thinning stage processing of fingerprint identification from analyzing of algorithm cycle distribution. A thinning algorithm changes a binary fingerprint image to one pixel width. Even though a thinning operation is very simple, it occupies very much cycle of microprocessor system. Hardware processing is more effective than software algorithm in speed, because a thinning algorithm is iteration of simple

instructions. The cycle distribution of each algorithm step is analyzed in FPGA and ARMulator environment.

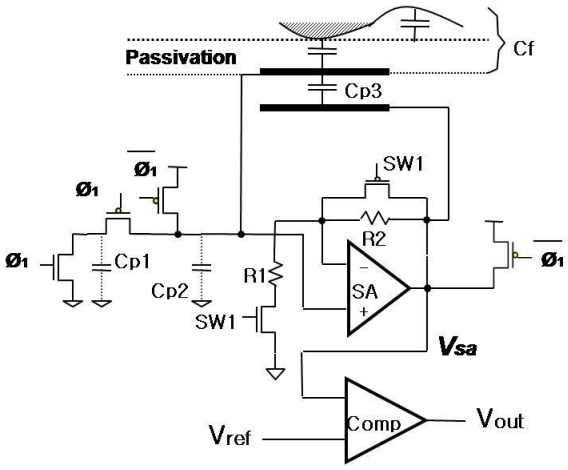
The rest of this paper is organized as follows. Section 2 discusses the typical and modified circuit design of a pixel level fingerprint sensor. Section 3 analyzes the cycle distribution of fingerprint verification algorithm using FPGA and also performs the RTL implementation of tinning algorithm. It is analyzed through the detailed simulation results for the proposed sensor system. Section 4 concludes the paper.

2. Fingerprint Sensor Design

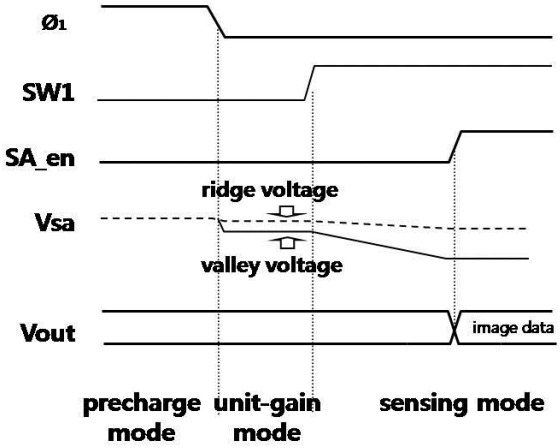
2.1. Typical sensing scheme

Figure 3 shows a conventional capacitive charge-sharing sensing scheme and timing diagram [3, 4]. The finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode. These two electrodes are separated by the passivation layer of the silicon chip and air. The series-connected capacitor Cf is composed of a capacitor between the metal plate and chip surface and another one between the chip surface and the finger skin. The capacitance of Cf is at its maximum value when a ridge has contact with the passivation layer. As the distance between the chip surface and the finger's skin increases, the capacitance becomes smaller. The variation of capacitance is transferred to output voltage by sensing scheme. The comparator discriminates a ridge and valley by reference voltage, Vref.

In Figure 3, "SA" is a unit-gain buffer and "Comp" is a comparator. When Ø1 is high and SW1 is low, the operation is in the precharge phase. The node Cp2 and Vsa are precharged to VDD, and node Cp1 is discharged to GND. In this phase, no charge is accumulated in Cp3 because the two electrodes have the same potential. In Cp2 and Cf, the amount of charge stored is Cp2•VDD and Cf•VDD. At the beginning of the unit-gain phase, the charges are redistributed between the nodes. The SW1 is low and R1 and R2 do not operate. The SA is enabled as a unit-gain buffer in this phase. The SA tracks the voltage change of the node Vsa, which makes the potential of Cp3 to zero. Usually, because Cp1 and Cp2 are the parasitic metal routing capacitances, they are much smaller than Cp3. Therefore, the adoption of SA is an effective method to remove the influence of Cp3. In the sensing phase, SW1 is high and SA operates as an attenuator by R1 and R2 ratio. Figure 4 shows an equivalent circuit of SA at the sensing phase. The SA is composed of only five MOSFETs for the restricted pixel area below the sensor plate. R1 is 5k and R2 is 1.4 k. The comparator 'Comp' is enabled by the signal 'SA_en' and compares the voltage of Vsa with the external reference voltage Vref. Thus, a binary output according to the finger pattern is produced. SA operates as an attenuator as well as a unit-gain buffer by handling the switching signal, SW1.



(a) Sensing circuit



(b) Timing diagram

Figure 3. Conventional capacitive charge-sharing sensing scheme

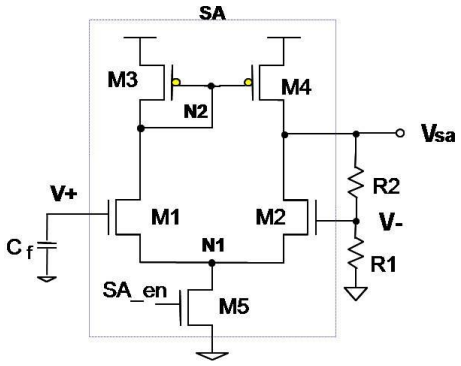


Figure 4. Equivalent circuit of SA in sensing phase

The operation and power consumption can be seen by the HSPICE simulation of the cell with condition of 40MHz, 0.35μm typical parameter and 3.3V power supply in

Figure 5. The voltage difference between the contacted point (ridge) and the non-contacted point (valley) is only 610mV in unit-gain phase, but 1720mV after sensing phase. Thereby, the comparator easily discriminates a ridge and valley. But, even though the voltage difference increased, there is power consumption by the static current. It is caused by the unit-gain buffer and feedback resistors. In sensing phase, when the valley voltage-Vsa starts to decrease by feedback resistors, the voltage cannot decrease fast enough. Because the conventional scheme has to wait for high state of SA_en until Vsa is 0 volt, the duration of static current is long. The average current is 605 uA in a ridge and 204 uA in a valley at 3.3V, 40MHz operation condition. If the occurrence number of a ridge and valley is same, the average current is 404 uA.

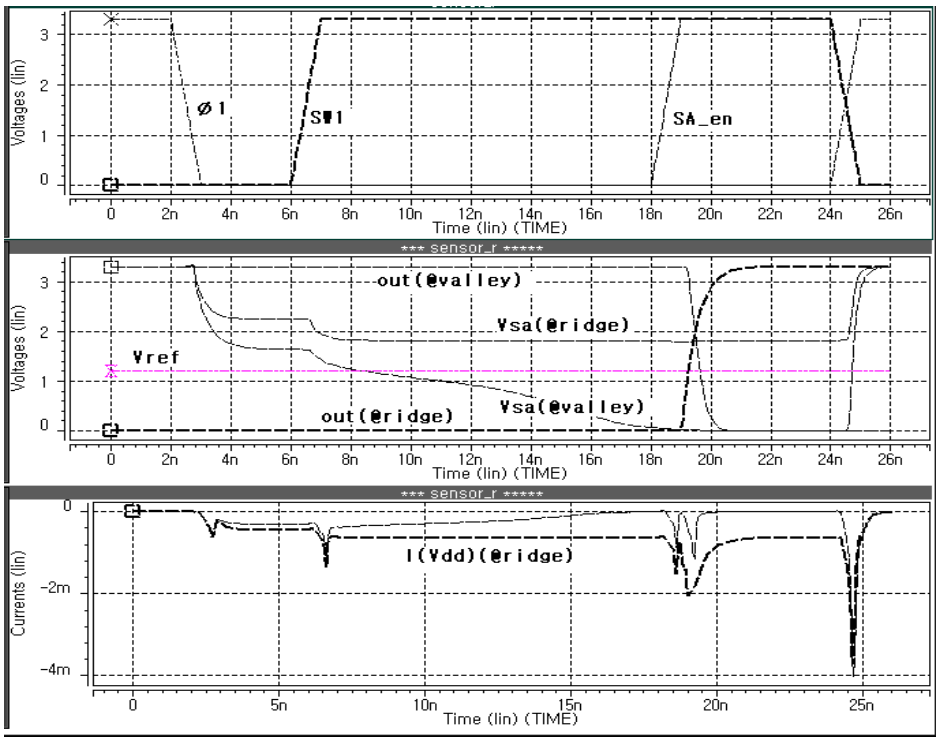
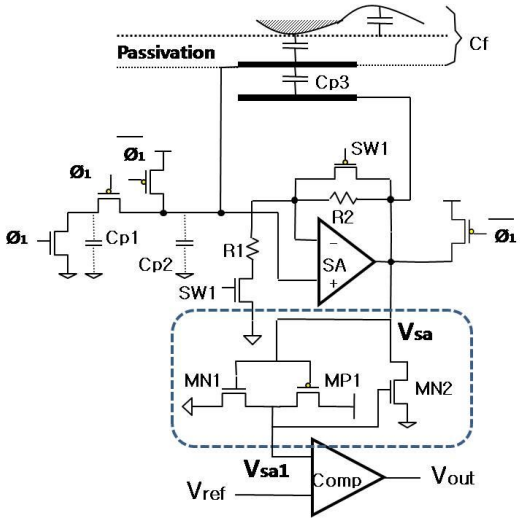


Figure 5. Simulation result of conventional circuit (3.3V, 0.35 μm CMOS process typical condition, 40MHz)

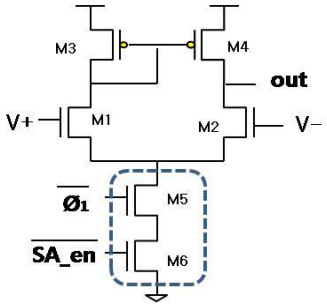
2.2. Proposed sensing scheme

Figure 6 shows the proposed capacitive sensing circuit. To accelerate fast sensing of the voltage decrease of Vsa, we inserted 3T-inverter with a small size transistor MP1, MN1 and MN2 into conventional sensing configuration. The width of MN1 transistor is designed more than MP1. Therefore, the logic threshold voltage of the inverter is less than VDD/2 for fast pull-up of Vsa1 in a valley. As a result, we can make fast SA_en enable time as shown in figure 6(c). It means reduction of static current duration. M5 of Figure 6(b) removes an additional static current after decision of a ridge or valley. Figure 7 shows a simulation result of proposed sensing circuit at 3.3V, 0.35 μm CMOS

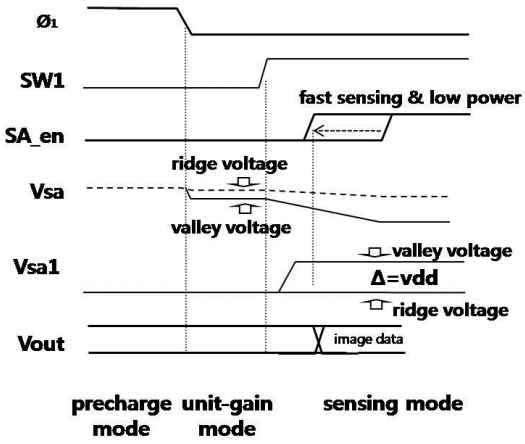
process typical condition, 40MHz. As the response of Vsa1 is fast, the duration of evaluation is reduced. The average current is 290 uA in a ridge and 142 uA in a valley. If the number of a ridge and valley is same, the average current is 216 uA. It means 47% reduction of power consumption than the conventional circuit. In proposed circuit, because Vsa1 is fully VDD in a valley and about 0 volt in a ridge, the voltage difference between a ridge and valley is about VDD in sensing phase. Our method produces about 90% improvement more 1720mV of conventional circuit in the voltage difference between ridge and valley. As a result, we can get a high-quality images without the influence of the reference volt(Vref). Figure 8 shows a layout of one pixel and the area is 58μm x 58μm. The image resolution is 423dpi.



(a) Proposed sensing circuit



(b) Proposed SA(unit-gain buffer)



(c)Timing diagram

Figure 6. Proposed capacitive charge-sharing sensing scheme

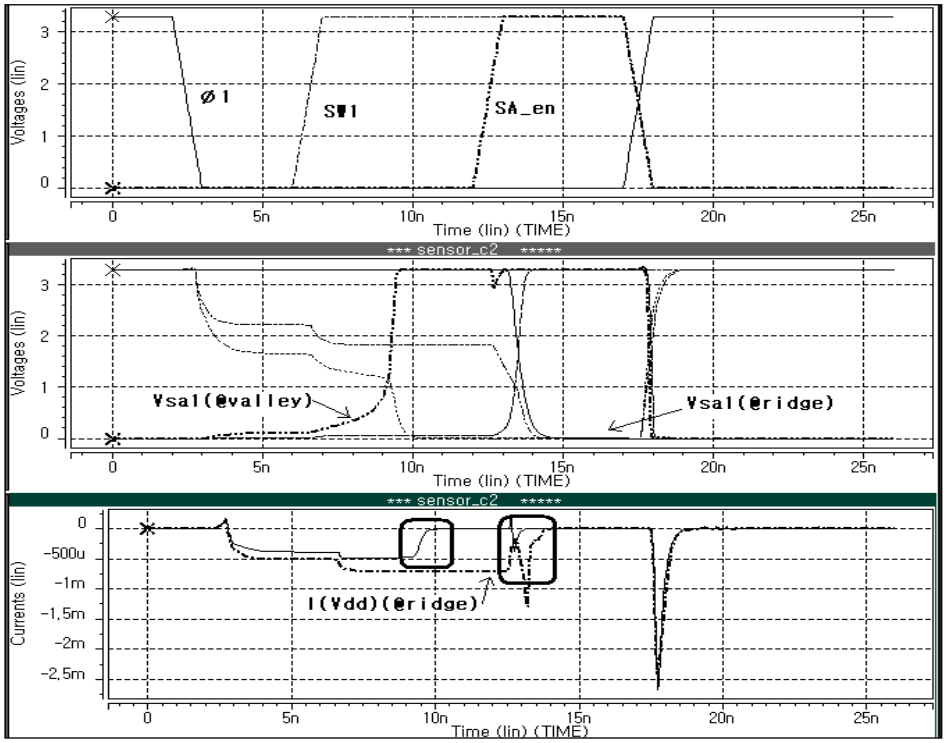


Figure 7. Simulation result of proposed circuit (3.3V, 0.35 μm CMOS process typical condition, 40MHz)

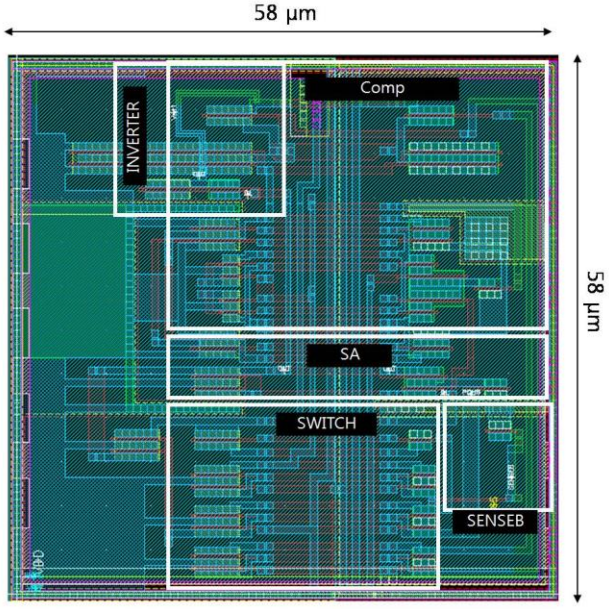


Figure 8. Layout of one pixel (58μm x 58μm, 0.35 μm CMOS process)

3. Identification Algorithm and Thinning Processor Design

Fingerprint image obtained from a fingerprint sensor has the image distortion and noise in it. Gabor filter is strongly recommended to get improved image and reduce a noise level [8]. It makes a smoothing image as shown in Figure 9. It made the image more effective to extract the minutiae from it. Before it is applied to the image, frequency and direction of the image should be calculated to emphasize unique features and make ridge clear. A one-pixel wide skeleton image is generated by changing thick ridge pattern to one-pixel line, which is called thinning stage as shown in Figure 9. Minutiae mean ridge ending or bifurcation of fingerprint images. After all the true minutiae of the image are detected, these features are stored in a pattern file.

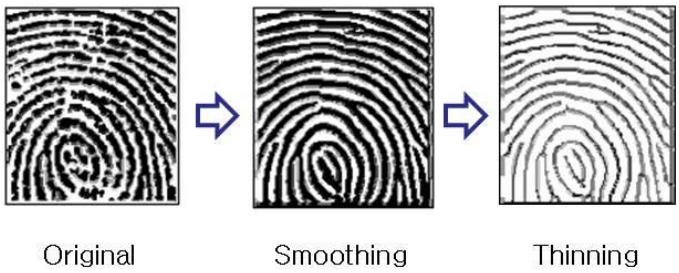


Figure 9. Fingerprint image preprocessing stages

This paper proposes an effective hardware scheme for thinning stage processing of a fingerprint identification based on minutiae from analyzing of algorithm cycle distribution. The cycle distribution of each algorithm step is analyzed in FPGA environment. Hardware processing is more effective than software one in speed, because a thinning algorithm is iteration of simple instructions. The hardware scheme is designed, and simulated in RTL. The logic was also synthesized by Synopsys Design Compiler using 0.35μm CMOS process. The layout is performed by an auto placement and routing tool.

3.1. Analysis of Algorithm

We implemented general purpose ARM7 compatible RISC microcontroller by FPGA to verify proper operation of the proposed fingerprint algorithm [7, 8]. Figure 10 shows the FPGA emulation board for verifying the algorithm. The design was composed of 3,336 slices(25%), 2,469 registers(9%), and 4,613 LUT(18%) with FPGA-XCV800Q240. The total equivalent gate count was 49,500 and the operating speed was 40MHz. We inserted the checkpoint routines at each step of the identification algorithm. The checkpoint routines successively turn on one of 8 LEDs on the emulation board. We finally confirmed that our embedded 32-bit RISC core successfully carried out the fingerprint authentication algorithm.

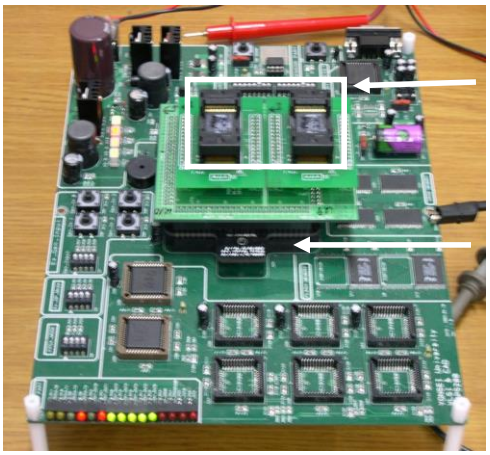


Figure 10. FPGA emulation board for verifying the algorithm

All the results of algorithm instructions are compared with those of ARMulator, which is a software emulator of the ARM processor, at every algorithm cycle as shown in Table 1 and Figure 11. The total clock number of our algorithm was 44.7M cycles and the operating speed was 1.1sec at 40MHz with a 160x192 sample image. GABOR filtering and thinning step occupied about 80% of total cycle. Minutiae detection time including matching is less then 3%. The thinning step occupies 39%(17.8M cycles). The processing time of thinning step is 0.446 second at 40Mhz. Here, QC: Quality Check, BO: Block Orientation, SBO: Smooth Block Orientation, RF: Ridge Frequency, FGF: Frequency Gaussian Filter, FLPF: Frequency LowPass Filter, GF: Gabor Filter T: Thinning, MD: Minutia Detection, DFM: Detect False Minutia, RM: Read Minutiae from a file, MP: Matching Processing, S-cycles: Sequential cycles. N-cycles: Non-sequential cycles. I-cycles: Internal cycles. C-cycles: Coprocessor cycles.

Table 1. Instruction cycle distribution

stage	QC	BO	SBO	RF	FGF	FLPF	GF	T	MD	DFM	MP	No. of clock
instruction	215059	1,375,079	253,535	2,918,970	13,029	107,652	12,496,058	9,548,256	552,487	443,587	81,920	27,790,573
S-cycles	245781	1,414,353	304,618	2,873,557	14,461	114,166	12,838,764	9,602,337	667,456	489,315	112,700	28,431,727
N-cycles	61446	366,037	99,830	847,425	3,174	14,407	3,213,533	5,635,665	197,734	200,131	3,797	10,581,733
I-cycles	30721	429,333	34,733	487,788	2,365	5,023	2,250,996	2,597,056	71,698	100,584	7,972	5,987,548
C-cycles	0	0	0	0	0	0	0	0	0	0	0	0
Total	337,948	2,209,723	439,181	4,208,770	20,000	133,596	18,303,293	17,835,058	936,888	790,030	124,469	45,001,008
%	0.75%	4.91%	0.98%	9.35%	0.04%	0.30%	40.67%	39.63%	2.08%	1.76%	0.28%	100.00%
clock	Total processing time(sec)											
40Mhz	0.008	0.055	0.011	0.105	0.001	0.003	0.458	0.446	0.023	0.020	0.003	1.125

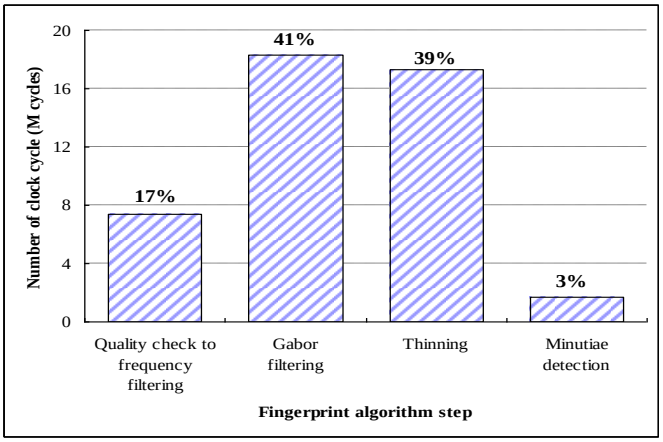


Figure 11. Instruction distribution graph

3.2. Thinning processor design

A thinning algorithm changes a binary fingerprint image to one pixel width. Even though a thinning operation is very simple, it occupies very much cycle of microprocessor system. Hardware processing is more effective than software algorithm in speed, because a thinning algorithm is iteration of simple instructions. In the past several decades, many thinning algorithms have been developed. In order to reduce the quantity of information minimally, a thinning algorithm play an important role in recognition of fingerprint images. The well-proved thinning algorithms are ZS(Zhang and Suen)[9]. ZS parallel thinning algorithm performs sub-iteration step twice in 3x3 image pixel window as shown in Figure 12. Here, P(i) and P1-8 are pixel binary image value. The value 1 means black and 0 means white.

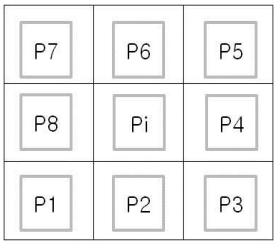


Figure 12. P(3x3): window pixel array

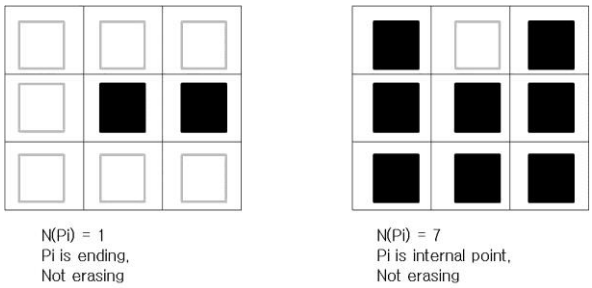


Figure 13. Number of black pixel neighbor P(i)

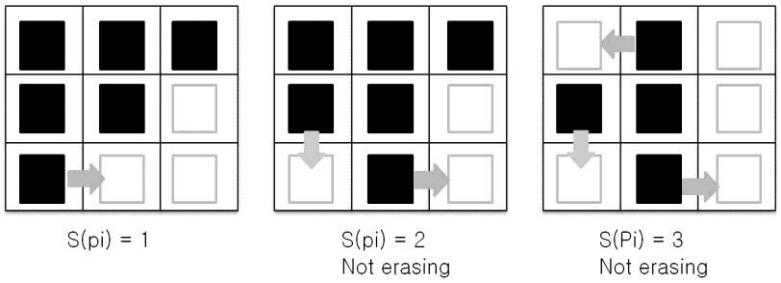


Figure 14. Number of black to white change neighbor P(i)

The first step: The pixels satisfied with following conditions are erased.

$$2 \leq N(Pi) \leq 6 \text{ and } S(Pi) = 1 \text{ and } P2*P6*P8=0 \text{ and } P4*P6*P8=0$$

Here, N(Pi) is the number of value 1 in 8-neighbor pixels of Figure 13 and expressed in following equation (1).

$$N(Pi) = P1 + P2 + \cdots + P8 \qquad (1)$$

And, as shown in Figure 14, S(Pi) means the number of 1 to 0 (1→ 0) patterns in 8-neighbor pixels.

The second step: The pixels satisfied with following conditions are erased.

$$2 \leq N(Pi) \leq 6 \text{ and } S(Pi) = 1 \text{ and } P2*P4*P8=0 \text{ and } P2*P4*P6=0$$

Iterations of 160x192 pixel array are performed based on the ZS algorithm in FPGA environment to verify proper operation. Figure 15 shows the proposed thinning processor block diagram. The 160x192 counter generates 2 dimensional address for selecting fingerprint pixel array. The 3x3 pixel window gen block generates 8-neighbor pixels of P(i,j) for 3x3 window. The thinning stag-1 and 2 blocks process first and second steps of ZS algorithm, respectively.

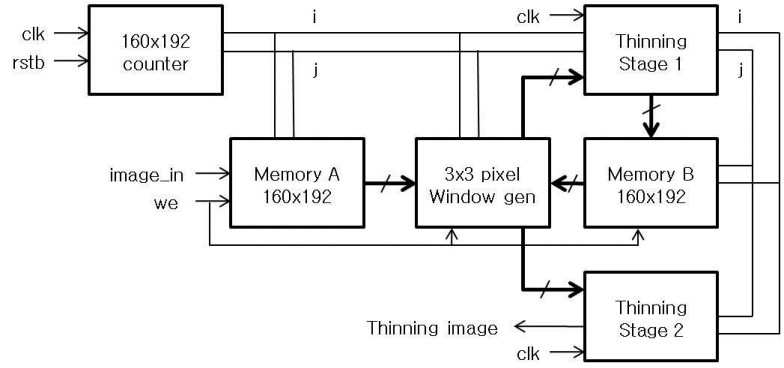


Figure 15. Block diagram of thinning processor

The RTL code of the ZS thinning algorithm was described by Verilog-HDL and synthesized by Synopsys Design Compiler using 0.35μm model. To confirm the operation of the proposed thinning processor, we extracted each parasitic capacitance from the optimized layout and performed the post-simulation on condition of 0.35μm worst. Figure 16 shows logic simulation result. The simulation was completed at 65000 clock cycles, while step 1 and 2 processing.

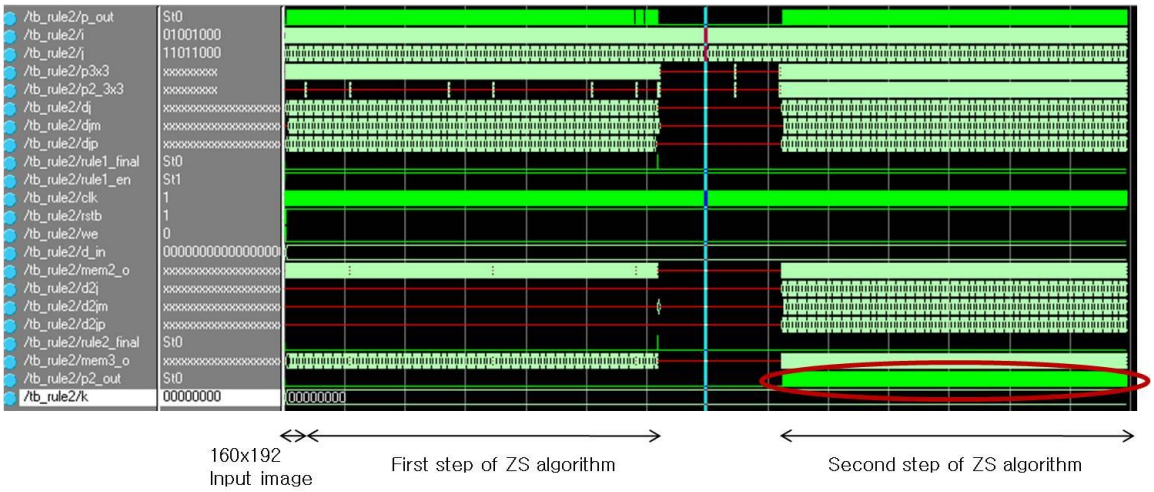


Figure 16. Logic simulation result

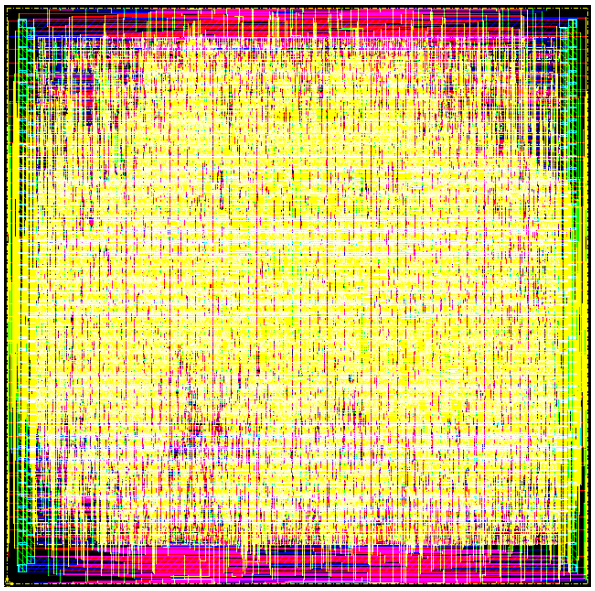


Figure 17. Layout of thinning processor (0.541 mm2 at 0.35μm CMOS process, 4-metal)

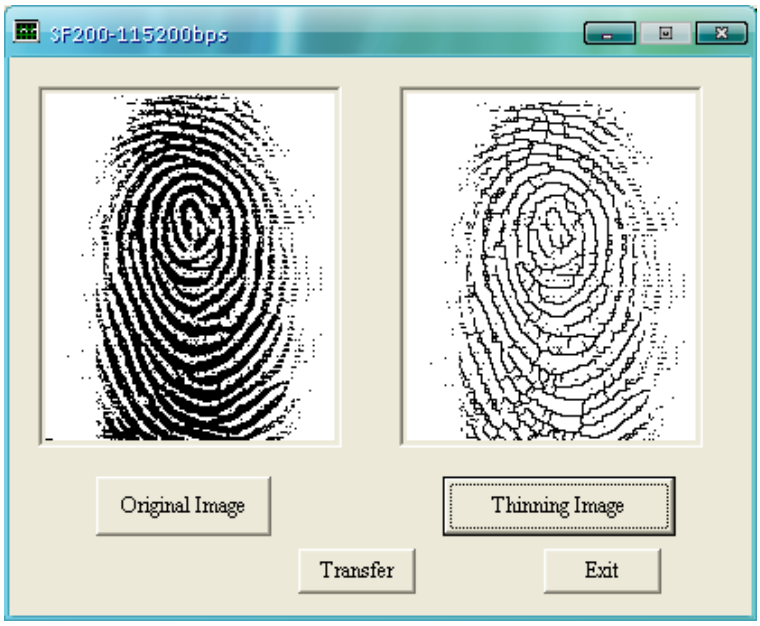


Figure 18. 160x192 sample image post-simulation result

Figure 17 shows the layout of thinning processor in 0.35µm CMOS process with 4-metal using an auto placement and routing tool. Area is 739µm x 732µm (0.541 mm^2) and gate count is 10,222 without memory. Therefore, the burden of chip area is small relatively in respect of 39% speed improvement. Figure 18 shows the thinned image of 160x192 pixel sample. The left image is original sensor output data and right is simulation output of thinning processor. The result shows the proposed thinning processor can successfully perform a fingerprint verification algorithm in ASIC.

The processing time of thinning step 1 and 2 is 16.2ms at 40MHz by total 65000 clock cycles. It means a thinning processing time can be reduced from about 400ms of a conventional system to 16.2ms, dramatically. Hardware burden will be relatively small on ASIC chip.

3.3. Circuit integration and system

Figure 19 and 20 describes the improved fingerprint system architecture including thinning processor. The result shows the proposed thinning processor can successfully perform a fingerprint verification algorithm in ASIC. We expect maximum 39% improvement of algorithm speed, replacement 32bit CPU by 16 or 8bit CPU, of low power consumption and small size fingerprint. It is our future work and will be implemented in FPGA or ASIC for a System on Chip(SoC)..

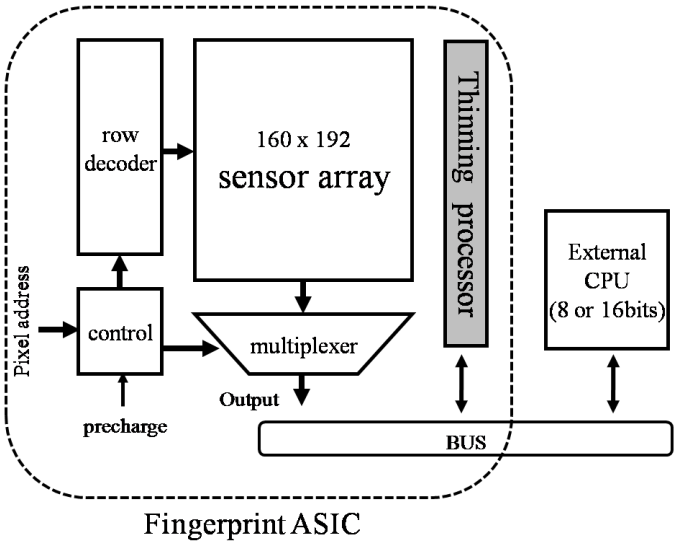


Figure 19. Integration of fingerprint sensor and thinning processor

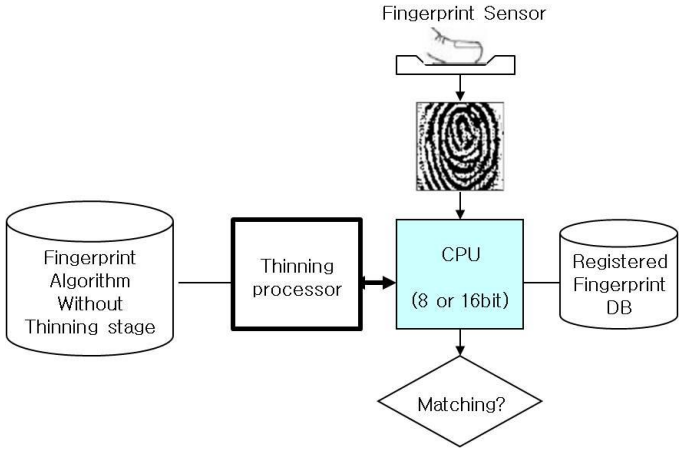


Figure 20. Operating flowchart of the proposed fingerprint system

4. Conclusion

This paper proposes the modified scheme of capacitive charge-sharing fingerprint sensors for low power consumption. The conventional sensing scheme minimizes the influences of internal parasitic capacitances and amplifies the voltage difference between the contacted point and the non-contacted point. Even though the voltage difference is increased, there is power consumption by the static current. It is caused by the unit-gain buffer and feedback registers configuration. The average current of one pixel was 404 uA in general operation. The modified capacitive detection circuit of charge sharing scheme includes the logic gate with a small size transistor to accelerate fast sensing of comparator. It means reduction of static current duration. In addition, because sensing voltage of a valley is fully VDD and about 0 volt in a ridge, the voltage

difference between a ridge and valley is about VDD. Proposed circuit reduces the static power dissipation and also increases the voltage difference between a ridge and valley more than conventional circuit. The modified detection circuit is designed and simulated in a 0.35 μm standard CMOS process, 40MHz frequency condition. The result shows about 47% power dissipation reduction and 90% improvement of difference between a ridge and valley sensing voltage.

In this paper, we also propose an effective hardware unit for thinning stage processing of a fingerprint identification algorithm instruction cycle distribution. Each step of a fingerprint algorithm is analyzed based on FPGA and ARMulator. A thinning stage occupies 39% cycle of 32-bit RISC microprocessor system for a fingerprint identification algorithm. Hardware processing unit is more effective than software processing, because a thinning algorithm is iteration of simple instructions. The ZS algorithm was applied. The hardware scheme was designed and simulated in RTL. The logic was also synthesized. The layout was performed based on an auto placement and routing in standard 0.35μm CMOS process. Area was 739μm x 732μm (0.541 μm2) and gate count was 10,222 without memory. The post-simulation result shows the proposed thinning processor can successfully perform a fingerprint verification algorithm in ASIC. We expect maximum 39% improvement of algorithm speed and replacement 32bit CPU by 16 or 8bit CPU, low power consumption and small size fingerprint system from the result.

Acknowledgements

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