International Journal of Multimedia and Ubiquitous Engineering
Vol. 10, No. 1 (2015), pp. 255-264
http://dx.doi.org/10.14257/ijmue.2015.10.1.25

Improved Design of Low Noise Amplifier

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Abstract

This paper addresses Low Noise Amplifier design which is also known as LNA for any application in wireless communication system. LNA is a very important part in RF receiver because when using a LNA noise can reduced by the gain by the amplifier when the noise of the amplifier is received directly from received signal. The low noise amplifier have designed to get the better performance by follow the requirement in this new era consists of high gain, low noise figure, lower power consumption, small chip area, low cost and good input and output matching. It is also used for excellent input and output matching and has a potential to get a lower noise. While for active inductor, is used to obtain the lower power consumption and to reduce the chip size in layout design.

Keywords: *active inductor, CGLNA, small area*

1. Introduction

Low noise amplifier also known as LNA is a special type of electronic that widely used in wireless communication system. A LNA can be found in RF transmitter and receiver for the basic building block in communication system. Hereby, LNA is the very important part of the receiver because it is placed at the front of the receiver and act as an amplifier to amplify the received signals in order to works as an electronic amplifier to amplify the received signals in order to get the level that required with the minimum produced their own additional noise while radio receiver consists of amplifier, mixer and filter.

Furthermore the main function of LNA is to amplify a very low signal. This amplify is without adding noise to maintain the required signal to noise ratio at very low power level and for higher signal levels and also the receiver which is receiver sensitivity can be received when the amplification provides the first level. By using this LNA noise can be reduced by the gain and also by the amplifier while the noise of the amplifier is inoculated directly into the received signal.

In Figure 1 is shows that the basic of RF transmitter and receiver block diagram. It commonly used to modulate and demodulated the transmission of RF signal. The function of the transmitter is carry the signal whereas the RF receivers receives the signal Nowadays, the technology has been growing up from time to time and consumer demand requirement also has been grown up that followed the requirement in RF transmitter receivers such as low noise, high gain, low cost, smaller size and good input and output matching. In this proposed project, a design will be created in order to fulfil these requirements.

ISSN: 1975-0080 IJMUE

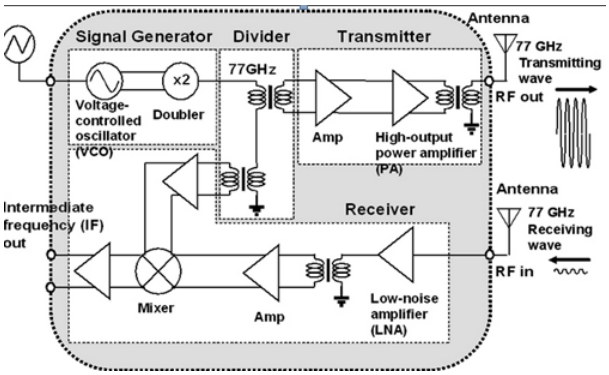


Figure 1. Block Diagram of RF Transceiver [1]

Low noise amplifier is the first stage in and it is very important part in RF receivers. Hereby, low noise amplifier should be matched with the antenna characteristic. The characteristic of antenna is excellent input and output matching and high gain.

To optimize the low noise amplifier design, the suitable topology should be selected for low power and low voltage. For shunt series feedback common source topology, it is difficult to trade of among gain, small noise figure and good input and output matching with very low power consumption. Furthermore for common gate topology, the gain less than 10dB with very low power consumption.

Next, the noise must add to the LNA because of the resistor thermal noise for resistor termination common source topology. Besides that, the specification is satisfies for inductive degeneration common source topology in very low power consumption but the isolation is not good enough compared to the cascade inductor source degeneration topology which can get the similar low noise amplifier performance with very low power consumption. Lastly, for cascade inductor source degeneration topology provides higher gain with a low noise figure [2].

Hence, there are several types fundamental of topologies low noise amplifier to choose a common low noise amplifier for optimized the LNA design. Figure 2 shows the topologies of LNA:

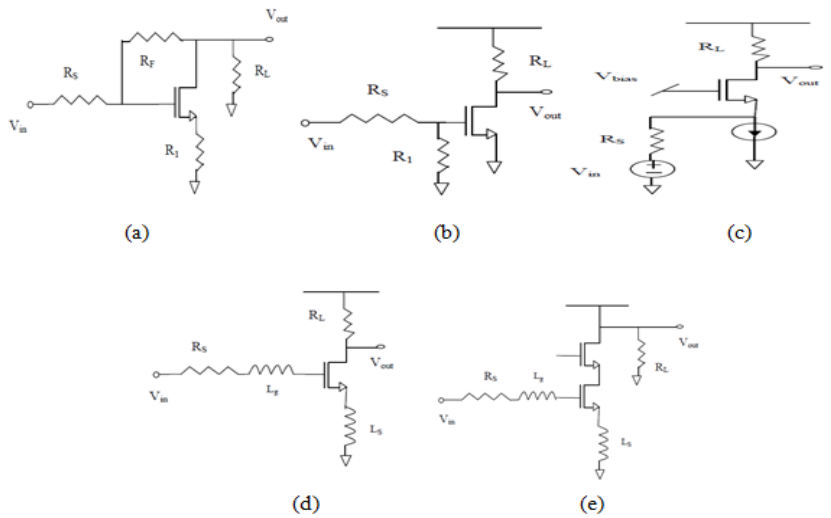


Figure 2. Fundamental of Topologies LNA:(a) Shunt Series Feedback Common Source (b) Inductive Degeneration Common Source (c) Common Gate (d) Resistive Termination Common Source (e) Cascode Inductor Source Degeneration[2]

2. Methodology

In this design there are mainly three stages in the proposed LNA. Every stage is explained in greater detail.

Figure 3. Block Diaram of Three Stages LNA[3]

1. Common Gate Amplifier

Basically, common gate amplifier is widely used in electronic field and one of three basic single stages field-effect transistor (FET) topologies. The advantages by using this FET are:

i. Used as current buffer or voltage amplifier.

ii. Used as input stage for LNA

iii. Obtain input impedance matching. The input impedance depends only on the trans-conductance of CMOS shown in equation 1

$$Z_{in} = \frac{1}{gm} \quad (1)$$

iv. Potentially has lower noise

2. Active Inductor

The active inductor has been implemented in this design which performs the same function as passive inductors. Active inductor is a combination of CMOS transistors. To design a low noise amplifier it has a fewer difficulty but it has higher flexibility to get the input and output matching, easy to design the layout and it does not have the magnetic field. For this design it does not used the real active inductor as main function but change it with transistor that perform the same function with active inductor. The advantages by using active inductor are:

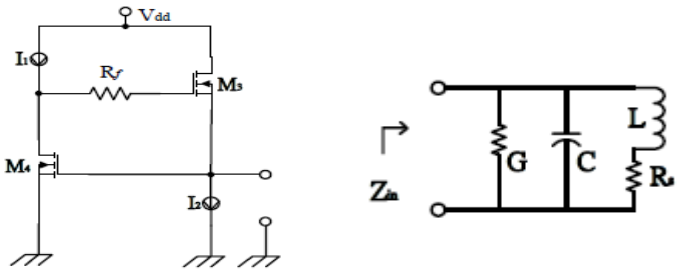
i. To get lower power consumption.

ii. Used to reduce chip area

iii. Used to reduce complexity

iv. Used to reduce cost

v. Used to compensate for the effect of parasitic capacitors at high frequencies Figure 4 shows the active inductor and its equivalent transistor circuit [3].



(a) (b)

Figure 4. Active Inductor Circuit and his Equivalent Circuit [3]

In Figure 4, the quality (Q) and inductance (L) and frequency (w) are calculated as follows:

$$Q = \sqrt{\frac{gm4\,gm3Cg3 \times (1 + Rfgds4)}{gds4^{2}Cg4}}$$

The quality factor is high enough because it depend on FR.

$$L \approx \frac{Cgs3(1 + Rfgds4)}{gm4\,gm3}$$

$$w = \frac{gm4\,gm3}{Cgs4Cgs3(1 + Rfgds4)}$$

After design is implemented with the equivalent circuit, it has been improved by using double feedback with second order. Figure 5 shows the active inductor after the improvement.

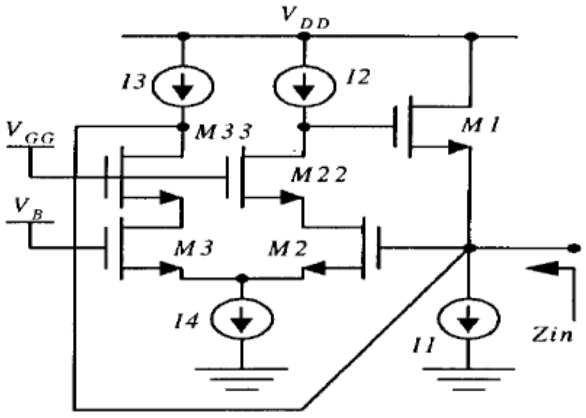


Figure 5. Double Feedback with Second Order Circuits [3]

3. Common Drain Amplifier

Common drain amplifier is one of three basic single-stages (FET) amplifier topologies also known as a source follower. Usually used as a voltage buffer. The advantages by using this FET are:

i. Used as a final stage in every LNA

ii. Capable to get small output impedance matching

iii. Potentially has lower noise

3. Background Studies

Based on the literature review, the comparisons of low noise amplifier design have been made to choose the appropriate schematic circuit for this project. From the comparison in Table 3, the first LNA design is found in [3] and has been choosen because of the best performance in term of the parameters that have been compared which is technology, gain (db), frequency (Ghz), noise figure (db), power supply, power consumption and area/ die size[4]. Table 1 show the comparison of the LNA design below:

Table 1. Comparison of LNA Design Studies

	Technology	Gain (dB)	Frequency (GHz)	Noise Figure (dB)	Power supply	Power consumption	Area/di e size
[3]	CMOS 0.18	20	2-3	3.1	1.8	0.5	0.003
[5]	CMOS 0.18	15.04	8.72	3.85	1.8	4.7	-
[6]	CMOS 0.18	17.04	5.8	3.1	1.8	6.4	-
[7]	CMOS 0.18	15.7 19.9	5.9 5.9	1.85 2.63	1 1	19.3 56.8	- -
[8]	CMOS 0.18	1.2	3.5	6.5	1.5	10.12	-
[9]	CMOS 0.18	14.3	2.4	1.6	1.8	0.9	-
[10]	CMOS 0.18	67.7	-	-	-	-	-
[4]	CMOS 0.18	19.5	5.2	2.7	3	-	-
[11]	CMOS 0.18	12-14	-	-	5.5-6	-	-
[12]	CMOS 0.18	-	2.4	2.17	-	-	-
[13]	CMOS 0.18	-	8.2	3.3-6.3	-	17.3	-
[14]	-	39.8	-	-	2.5	-	0.2

4. The Proposed LNA

From the comparison above, the proposed a low noise amplifier circuit had been selected based on the best performance in term of the noise figure, high gain and power consumption. The proposed a low noise amplifier circuit uses the active inductor by using the inductor less to achieve the requirements. In addition it is implemented with latest CMOS technology 0.13µm.

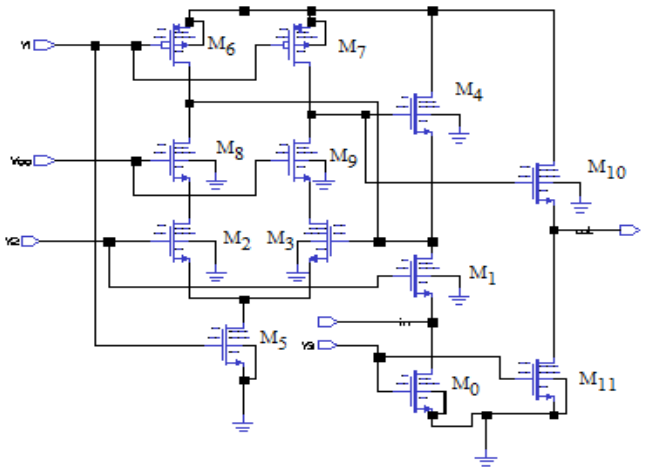


Figure 6. Schematic of the LNA to be Improved [3]

This circuit in Figure 6 will be improved. This design will involve a change in the CMOS technology from 0.18µm to 0.13µm. Furthermore the transistor size will also be changed.

Table 2. Transistor Width [3]

Transistor	Width
M0	8 um
M1,M2,M3	12 um
M4,M5	1.8 um
M6,M7	2 um
M8,M9	4 um
M10	3.6 um
M11	2.7 um

The new improved design should meet the requirements in Table 3.

Table 3. Specification of LNA design [6]

Parameter	Specification
Supply Voltage	1.8V
Gain	>10dB
Noise Figure	<3dB
Power Consumption	<50mW
DC current	<20mA

5. Results and Discussion

An improved low noise amplifier is designed and simulated by using CADENCE software with latest technology 0.13µm. The DC biasing voltage values for V1= 1.1, V2=0.6, V3=0.6 and Vgg=0.7.

In this new design the ratios (W/L) of the transistor that used in this circuit have been modified. For the transistor lengths the ratio is 0.13µm for all transistors while the transistor width the ratios are different by using the manual calculation. Figure 7 shows the schematic circuit of the proposed LNA design and Table 5 shows the transistor ratio after enhancement.

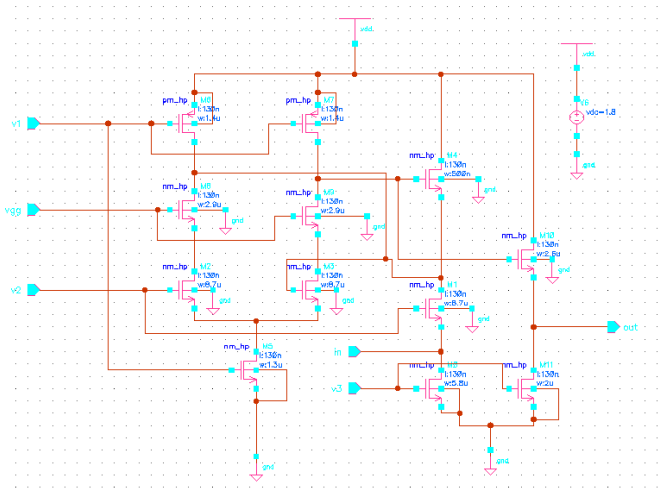


Figure 7. Schematic of the New Improved Low Noise Amplifier

Table 4. The New Size of Used Transistor

Transistor	Width	Length
M0	5.8um	0.13um
M1,M2,M3	8.7um	0.13um
M4	0.5um	0.13um
M5	1.3um	0.13um
M6,M7	1.4um	0.13um
M8,M9	2.9um	0.13um
M10	2.6um	0.13um
M11	2um	0.13um

While completing the design, there is major challenges arise of producing the right value of gain. On the first experiment, all the transistors are combined into one ground nodes. The result shows that, gain value is negative. So, it does not meet the requirement of gain which it must be in positive value. Then it proceeds to second experiment. The ground nodes are connected to each transistor respectively. Based on these experiments, it can be concluding that the ground nodes cannot be combined because of the input DC biasing value for each transistor is different. Figures 8 and 9 shows the gain in negative value and positive value.

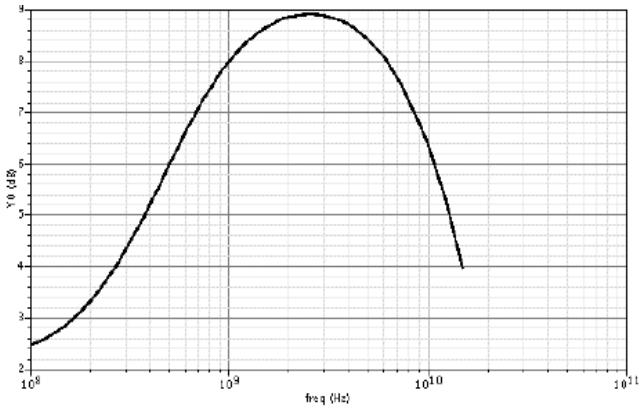


Figure 8. Gain in Negative Value

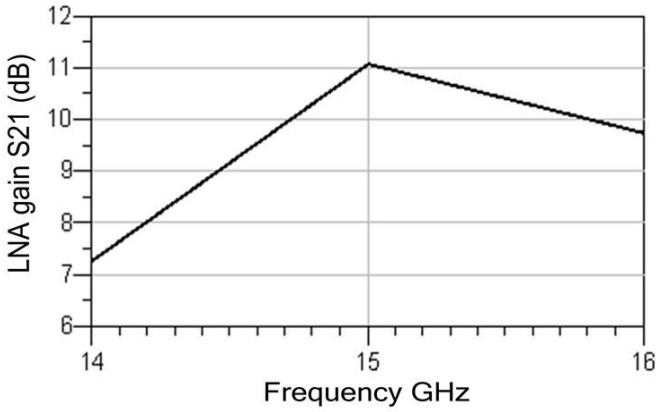


Figure 9. Gain in Positive Value

The best design for low noise amplifier is capable to achieve the highest value of gain and it have to be more than 10dB based on the specification of LNA design [6]. An adjustment has been made to the value of DC bias. After few trials the highest gain is successful achieved is 15.2dB. In order to get this value, the Vgg decrease to 0.5v while V1 is increased to 1.2 and the rest are remaining. The transistor width for M4 also changes to the 0.5µm. Table 4 shows the analysis that have been made to get gain in positive value.

Table 5. Analysis of Gain Value

Vgg	V1	V2	V3	Gain(dB)
0.5	1.2	0.6	0.6	11.39
0.7	1.1	0.6	0.6	9.22
0.4	1.1	0.6	0.6	-23.9
0.5	1	0.6	0.6	-30.63
0.5	1.3	0.6	0.6	10.9
0.5	1.4	0.6	0.6	11.86
0.5	1.5	0.6	0.6	11.56
0.5	1.5	0.7	0.6	4
0.5	1.5	0.5	0.6	7.753
0.5	1.5	0.5	0.7	4.48
0.5	1.5	0.5	0.5	-31
0.4	1.2	0.7	0.6	-2

Mainly, the transient analysis is very important to the amplifier. It is because from this analysis it can prove that this design is amplifier or not. The function of the amplifier is to amplify the output signal from the input signal. Therefore, to prove that this design is amplifier or not the output signal must greater than the input signal. Figure 10 shows the simulation of transient analysis.

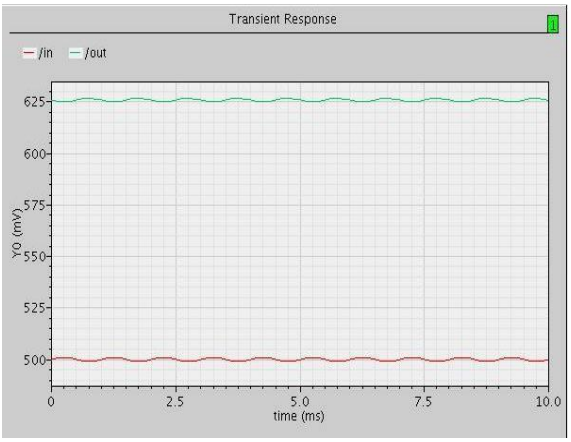


Figure 10. Transient Analysis Simulation

After transient analysis is done, the AC analysis for LNA design is obtained. To achieve the desired specifications gain, optimum transistor width, input value of DC biasing voltage was the main criteria for design of LNA [5]. When high gain has been achieved the noise can be reduce by gain by amplifier that captured by antenna. To obtain gain of the LNA design, it can use from this expression below:

$$Gain = 20\log_{10}\left(\frac{V_{out}}{V_{in}}\right)$$

For this design the gain is successful achieve of 15.2dB based on the design specification. Figure 11 shows the simulation result of gain in AC analysis.

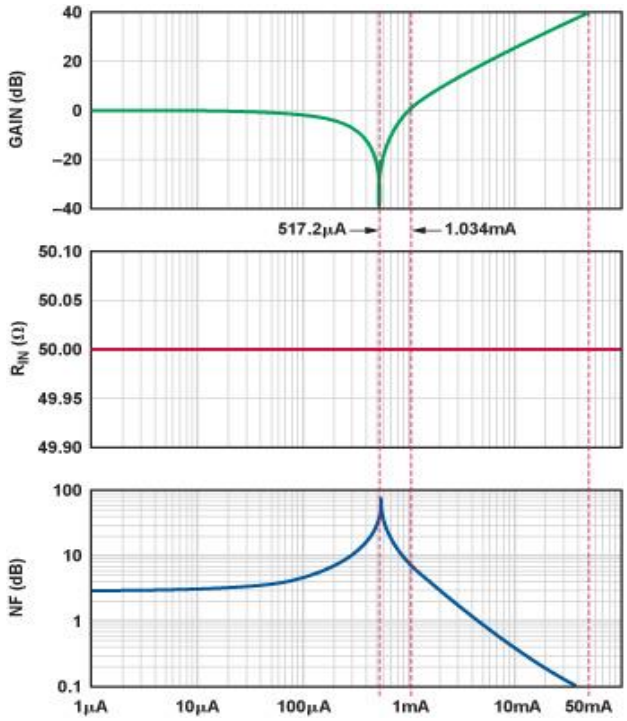


Figure 11. AC Analysis Simulation

6. Conclusions

A new improved design of LNA has been proposed. The new design achieved a gain of 15.2dB, a noise of 7dB, extremely low power consumption of 0.8mW, good input and output matching and small chip size of 0.26mm². However it possesses noise issue due to the usage of the latest technology which is 0.13µm.

References

[1] P. Kavyashree and S. S. Yellampalli, "The Design of Low Noise Amplifiers in Nanometer Technology for WiMAX Applications", M.Tech(VLSI Design), VTU Extension Centre, UTL Technologies Limited Bangalore, India, vol. 3, no. 10, **(2013)**, pp. 1–6.
[2] S. Kumar, "CMOS Low Noise RF Amplifier Design and Parameter Estimation using ANN", Master of Technology in VLSI Design &CAD, vol. 147004, **(2012)**.
[3] N. Moser, S. J. Rogers, P. Supervisor and J. Rogers, "ELEC 4907 – Fourth Year Engineering Project Final Report A 5.2 GHz Differential Cascode Low Noise Amplifier", **(2004)**.
[4] P. Version, "Low Noise Amplifier Design Measuremants", Inc., 555 Riber Oaksparkway, San Jose, CA 9514, USA, Product Version 5.0, **(2004)**.
[5] N. Rani and S. Sharma, "Design of Low Noise Amplifier at 3-10GHz for Ultra Wideband Receiver", International Journal of Innovation Research in Computer and Communication Engineering, vol. 1, no. 7, **(2013)**.
[6] P. Kavyashree and S. S. Yellampalli, "The Design of Low Noise Amplifiers in Nanometer Technology for WiMAX Applications", M. Tech (VLSI Design), VTU Extension Centre, UTL Technologies Limited Bangalore, India, vol. 3, no. 10, **(2013)**, pp. 1–6.
[7] P. G. Afshar, "International Journal of Advanced Research in A 3.5 GHz Low Noise Figure Mixer with High Conversion Gain for WiMAX Systems", IEEE of Advanced Research in Compuetr Science and Software Engineering, vol. 3, no. 5, **(2013)**, pp. 695–699.
[8] B. Liu, C. Wang, M. Ma and S. Guo, "An Ultra-Low-Voltage and Ultra-Low-Power", School of Computer and Communication, Hunan University, China vol. 18, no. 4, **(2009)**, pp. 527–531.
[9] A. Goel and G. Singh, "A Novel Low Noise High Gain CMOS Instrumentation Amplifier for Biomedical Applications", Centre for Development of Advanced Computing (C-DAC), Mohal, India, vol. 3, no. 4, **(2013)**, pp. 516–523.

[10] C. George and J. Rogers, "Design of Broadband Low Noise Amplifier for use in a Cable Tuner", Final project Report, vol. 51, no. 2, **(2014)**, p. Contents2.
[11] E. D. Link, "CMOS LNA Design for Multi-Standard Application", Master Thesis at Electronic Devices Linkopings Institute of Technology, **(2006)**.
[12] S. S. Kim, Y. S. Lee and T. Y. Yun, "High-Gain Wideband CMOS Low Noise Amplifier with Two-Stage Cascode and Simplified Chebyshev Filter", ETRI J., vol. 29, no. 5, **(2007)**, pp. 670–672.
[13] R. R. Harrison, C. Charles and S. Member, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications", IEEE Journal of Solid-State Circuits, vol. 38, no. 6, **(2003)**, pp. 958–965.

