International Journal of Bio-Science and Bio-Technology
Vol.6, No.5 (2014), pp.55-66
http://dx.doi.org/10.14257/ijbsbt.2014.6.5.07

Design of CMOS Two-stage Operational Amplifier for ECG Monitoring System Using 90nm Technology

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Abstract

This paper presents a high performance Two-stage operational amplifier for biomedical applications. This Two-stage is designed for low noise, low power, high PSRR and high CMRR. The Miller compensation technique (Cc) is used with a nulling active resistance (Rz) implemented using Transmission gate transistors for stable operation in feedback mode. The operational amplifier was manufactured in a SPECTRE using GPDK 0.90-um CMOS technology with threshold voltages of a 0.17 V and - 0.14 V achieve a low power 2.6uW, high CMRR up to 130dB and PSRR up to 70dB at 1V power supply.

Keywords: *Two-stage amplifier, Miller compensation, Transmission gate, CMRR (Common mode Rejection Ratio)*

1. Introduction

The trend in the use of low-voltage power supplies for CMOS integrated circuits is by the reliability issue of small size MOSFET transistors and the increasing use of low-weight long life battery-operated portable electronic systems [1, 2].

With the rapid development of microelectronics in the recent past years, more and more applications require an ultra-low amplitude signal measurement module, such as implantable devices in biomedical application to monitor several Neuro-muscular activities [3-6].

Monitoring biomedical signals of the human body is a very interesting topic since it can be used to know vital health information of the body from the acquired data. These data capacitates medical practitioners to diagnose diseases [7, 8].

Biomedical signals, such as electrocardiogram (ECG), Electromyogram (EMG), Electroencephalogm (EEG), are characterized by their low voltage-levels and low frequency, Table 1 shows the characteristics of these signals [8 -12]

Table 1. Most Commonly used Biomedical Signals

Signal	Frequency	Amplitude
ECG	0.05-250 Hz	5 uV-8 mV
EEG	0.5-200 Hz	2 uV-200 uV
EMG	0.01-10 KHz	50 uV-10 mV

The Famous architecture used in a biomedical monitoring system, are an operational amplifier, must exhibit very low-referred noise, low power and high Common Mode Rejection Ratio (CMRR).

ISSN: 2233-7849 IJBSBT

In this paper, a low voltage, low noise and high CMRR operational amplifier for portable monitoring system is proposed. The operational amplifier is able to work under 1-V supply and has high CMRR.

2. ECG Data Acquisition System

ECG data acquisition begins with the use of electrodes that attached to body skin. Three electrodes are used as sensors to detect the heart signals from a human body. Two electrodes are placed each on the left and right wrist while the third electrode is placed on the ankle of the leg as ground [13].

The ECG signal that acquired is in the range of 5uV to 8 mV. Due to the weak voltage level, the signal is fed into an amplifier circuit to be amplified to a desirable voltage level. Output from the amplifier is then fed into a bandpass filter circuit and a High Q notch filter. The purpose of this filter is to filter out the very low and high frequency noise components of the signals and the 60-Hz power line interference. The desirable analog output from the filter is then sent to S/H and ADC to become a digital signal. After that, these digital data will processed in PCs or microprocessors. Figure.1 shows the proposed ECG data acquisition system [7, 13-16].

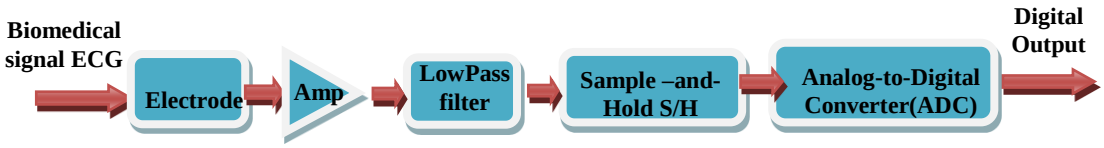

Figure 1. The Proposed ECG Data Acquisition

3. ECG Signal

Electrocardiogram (ECG) signal plays a vital role in the monitoring and diagnosis of the health conditions of the heart. An electrocardiogram is a recording of the small electric waves being generated during heart activity. The main tasks in the ECG signal analysis are the detection of QRS complex and the estimation of the instantaneous heart rate. Figure 2 shows an example of a normal ECG trace, which consists of a P wave, a QRS complex and a T wave.

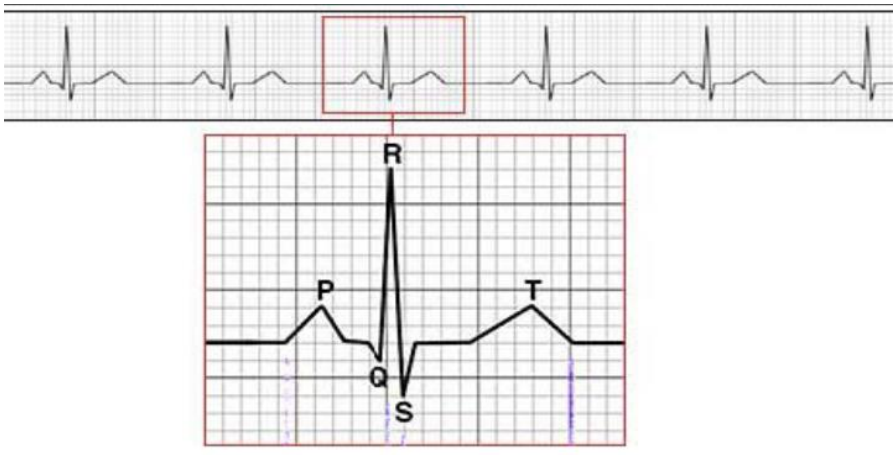

Figure 2. Shows an Example of a Normal ECG Trace

✓ The P wave represents the atrial contractions.
✓ QRS complex represents the ventricular contractions. The R peak indicates a heartbeat.

✓ The T wave is the last common wave in an ECG. This electrical signal is produced when the ventricles are re-polarizing.

The heart is a muscular pump made up of four chambers. The two upper chambers are called atria, and the two lower chambers are called ventricles. A natural electrical system causes the heart muscle to contract and pump blood through the heart to the lungs and the rest of the body [13].

We have collected data from MIT-BIH Arrhythmia Database [17-19], for training and testing of proposed ECG amplifier Design. See Figure 3 of the input (Vin) ECG signal.

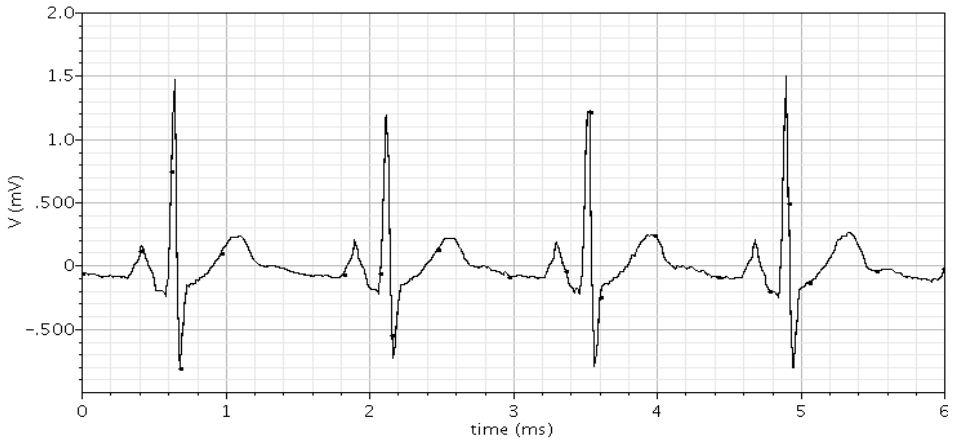

Figure 3. ECG Signal from MIT-BIH Arrhythmia Database.(Vin(max)=1.5mV)

4. ECG Amplifier Design

A normal ECG signal falls in the range of 5uV – 8mV. The amplifier is required to increase this weak signal into an acceptable level. The main operational amplifier for biomedical applications is illustrated in Figure 4. This Two-stage architecture with miller compensation capacitor (Cc) and nulling active resistor (Rz), is used for the design of the operational amplifier with the first stage being a differential input pair and the second, a gain stage. Because the Biomedical signal is so weak, the noise will affect the real biomedical signal. Due to the low frequency of biomedical signal the flicker noise dominates, it has strong dependence on the width and length product of a CMOS transistor. The flicker noise is modeled in Eq (1), the spectral density of flicker noise is inversely proportional to the transistor area, WL. In other words, 1/f noise can have a lesser effect on larger devices. However the input pair (M1 and M2) of the input stage has been designed using large PMOS transistors. A P-channel current source (M5) and an n-channel current mirror load (M3 and M4) are used in the input stage.

$$V_n^2 = \frac{K}{C_{OX}WL} \cdot \frac{1}{f} \quad (1)$$

The second stage of the operational amplifier includes an n-channel common-source amplifier (M6) with a p-channel current source load (M7).

The high output resistances of these two transistors (M7, M6) equate to a relatively large gain for this stage and an overall moderate gain for the complete amplifier. Because the operational amplifier inputs are connected to the gates of MOS transistors, the input resistance is essentially infinite. The sizes of the transistors were designed for a bias current of 0.5μA to provide for sufficient output voltage swing, output-offset voltage, slew rate, and gain-bandwidth product.

4.1. Current Mirrors

Current mirrors are used extensively in MOS analog circuits both as biasing elements and as active loads to obtain high AC voltage gain [20, 21]. Enhancement mode transistors remain in saturation when the gate is tied to the drain, as the drain-to source voltage (*VDS*) is greater than the gate-to-source voltage (*VGS*) due to the threshold voltage (*Vth*) drop, *i.e.*,

$$V_{DS} = V_{GS} - V_{Th} \quad (2)$$

Based on Eq (2), constant current sources are obtained through current mirrors designed by passing a reference current through a diode-connected (gate tied to drain) transistor.

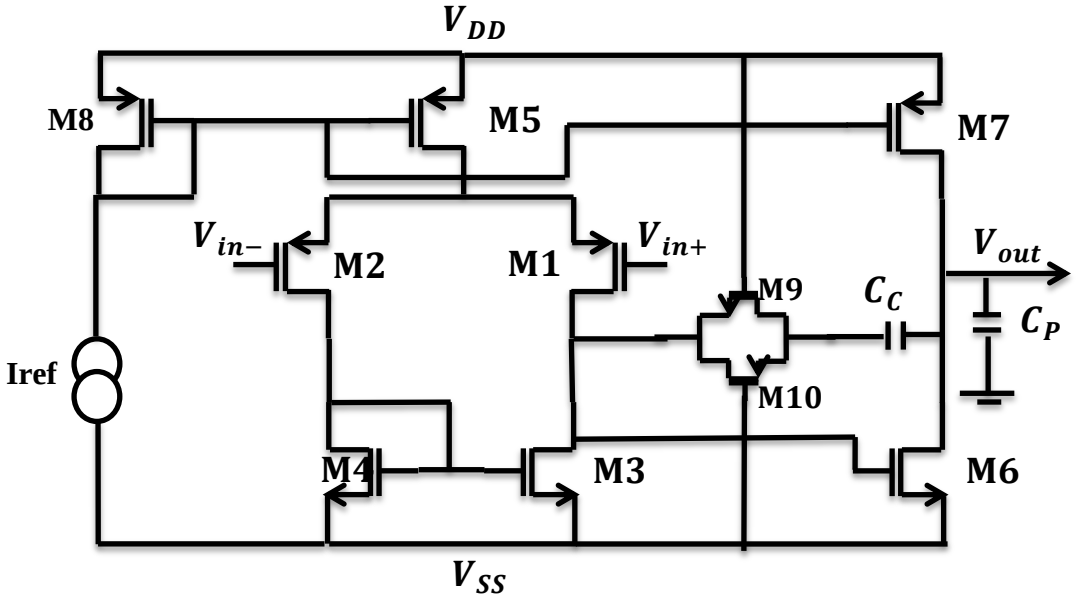

Figure 4. Schematic of Two-stage Operational Amplifier

We choose a simple current mirror because low voltage (1-V), Figures 5(a) and (b) show the PMOS and NMOS current mirrors design. A PMOS mirror serve as a current source while the NMOS acts as a current sink. The voltage developed across the diode-connected transistor is applied to the gate and the source of the second transistor, which provides a constant output current. Since both the transistors have the same gate to source voltage, the currents when both transistors are in the saturation region of operation, are governed by the following Eq (3) and Eq(4) assuming matched transistors. The current ratio Iout/Iref is determined by the

aspect ratios of the transistors. The reference current that was used in the design is 0.5μA. The desired output current is 1μA.

For the PMOS current mirror, we can write,

$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{W_7}{L_7}}{\frac{W_8}{L_8}} \quad (3)$$

For the NMOS current mirror, we can write,

$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{W_4}{L_4}}{\frac{W_3}{L_3}} \quad (4)$$

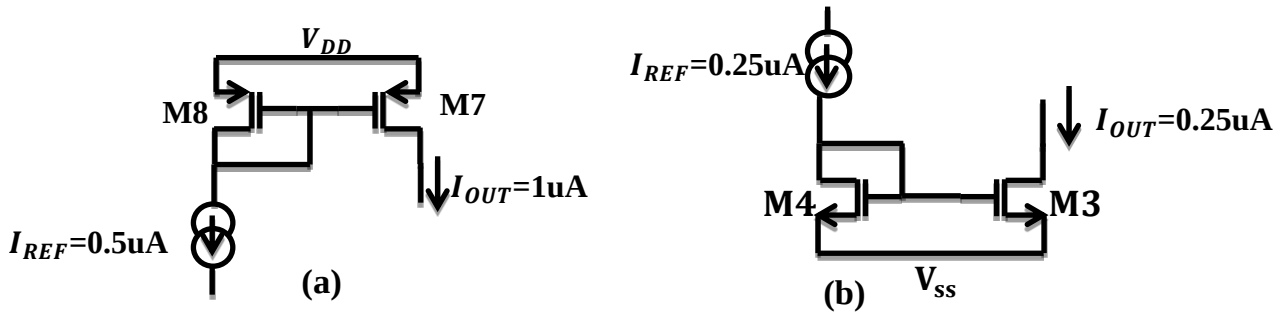

Figure 5. (a) PMOS Current Mirror, (b) NMOS Current Mirror

4.2. Active Resistors

There are two active resistors used in the design. Firstly, the reference current that is applied to the current mirror is obtained by means of an active resistor. The resistor here is obtained by simply connecting the gate of an NMOS (M11) to its drain as shown in Figure 6. This connection forces the MOSFET to operate in saturation.

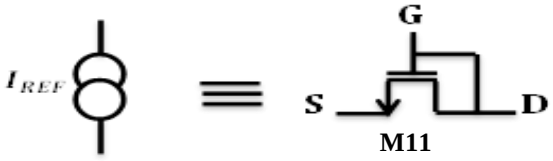

Figure 6. Active Resistor

The second active resistor a transmission gate (TG) shown in Figure 7 has been used to realize the nulling active resistance (Rz) to reduce the effects of the right hand plane zero in the transfer function. The gate of these transistors M9, M10 is biased at VDD, VSS respectively. Its small signal output resistance is obtained from Eq (5) and Eq(6) (V_{ds} very small).

The dynamic range limitations associated with single channel MOS switches can be avoided with CMOS switch shown in figure 7. Using the CMOS technology, a switch usually

constructed by connecting P-channel and N-channel enhancement mode in parallel as illustrated.

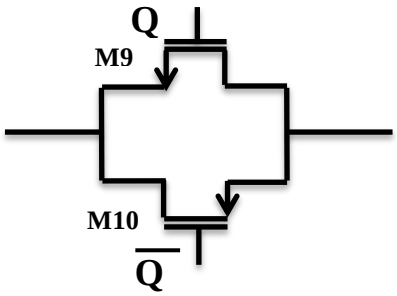

Figure 7. Transmission Gate (TG)

For this configuration, When Q is low, both transistors are off, creating an effective open circuit. When Q is high both transistors are on, giving a low impedance state. The bulk potentials of the p-channel and n-channel devices are taken at the highest and lowest potentials respectively. The primary advantage of the CMOS switch over the single channel MOS switch is that the dynamic analog-single range in the ON state is greatly increased [21].

$$R_{ON} = \frac{1}{U_n C_{OX} \frac{W}{L}(V_{GS} - V_{Thn})} \quad (5)$$

$$R_{OP} = \frac{1}{U_P C_{OX} \frac{W}{L}(V_{SG} - |V_{Thp}|)} \quad (6)$$

5. Results

5.1. Device Parameter

Table 2 gives the device parameter for a Two-stage operational amplifier.

Table 2. Device Parameter for Two-stage Amplifier

Device	Type	W(um)	L(um)
M1,M2	P	10	0.378
M3,M4	N	18	0.556
M5,M8	P	35	0.460
M7	P	80	0.530
M6	N	15	0.100
M9	N	1	0.100
M10	P	10	0.100
M11	N	3	0.800

5.2. Frequency Response, Compensation

Operational amplifier architectures are generally two types: single-stage externally compensated or two stage internally compensated amplifiers, both of which can have a dominant two pole type frequency response [21]. Ignoring higher order poles, the small signal behavior of the two stage amplifier can be modeled by the general two poles, one zero small signal equivalent circuit shown in Figure 8. Referring back to the model of the input stage Figure 4 (Without (Cc) and (Rz)), We have two poles these are Eq (7) and Eq (8)

$$P_1 = \frac{1}{C_1 \frac{1}{g_{m3}}} \quad \textbf{(7)}$$

$$P_2 = \frac{1}{C_2 (r_{02} r_{04})} \quad \textbf{(8)}$$

The compensation of the two stage CMOS amplifier can be carried out using a pole splitting capacitor. The goal of the compensation task is to achieve a phase margin greater than 45 degree. The circuit can be approximately represented by the small signal equivalent circuit of Figure 8 (without Rz), if the non-dominant poles which may exist on the circuit are neglected.

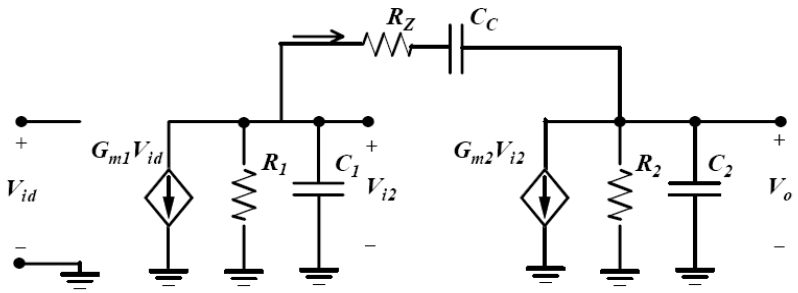

Figure 8. Simplified Small Signal Model of the basic Two Stage Op-amp Added with the Nulling Resistor

The circuit displays two poles and a half right plane zero, which under an assumption that the poles are widely separated can be shown to be approximately located at (Eq (9), Eq (10) and Eq (11)).

$$P_1 = \frac{-1}{(1 + g_{m2} R_2) C_C R_1} \quad \textbf{(9)}$$

$$P_2 = \frac{-g_{m2} C_C}{C_2 C_1 + C_C C_1 + C_2 C_C} \quad \textbf{(10)}$$

$$Z = \frac{g_{m2}}{C_C} \quad \textbf{(11)}$$

Note that the pole due to the capacitive loading of the first stage by the second, $p1$, has been pushed down to a very low frequency by the miller effect in the second stage, while the

pole due to the capacitance at the output node of the second stage *p*2, has been pushed to a very high frequency due to the shunt feedback. For this reason, the compensation technique is called pole splitting.

Physically, the zero arises because the compensation capacitor provides a path for the signal to propagate directly through the circuit to the output at high frequencies. Since there is no inversion in that signal path as there is in the inverting path dominant at low frequencies, stability degraded.

An even simpler approach is to insert an active nulling resistor (Rz) in series with the compensation capacitor as shown in Figure 4 and Figure 8. If *Rz* is assumed to be less than *R*1 or *R*2 and the poles are widely spaced, then the poles are: (Eq(12),Eq(13),Eq(14) and Eq(15)).

$$P_1 = \frac{-1}{(1+g_{m2}R_2)C_C R_1} \cong \frac{-1}{g_{m2}C_C R_1 R_2} \quad \textbf{(12)}$$

$$P_2 = \frac{-g_{m2}C_C}{C_1C_2 + C_CC_2 + C_1C_C} \cong \frac{-g_{m2}}{C_2} \quad \textbf{(13)}$$

$$P_3 = \frac{-1}{R_Z C_1} \quad \textbf{(14)}$$

$$Z = \frac{-1}{C_C(\frac{1}{g_{m2} - R_Z})} \quad \textbf{(15)}$$

The resistor RZ= (Ron||Rop) allows independent control over the placement of the zero. The zero vanishes when RZ is made equal to 1/gm2. In fact, the resistor can be further increased to move the zero into the left half-plane and place it on top of p2 to improve the amplifier phase margin. RZ can be realized by a CMOS switch transistor in the triode region.

Using CMOS switch is to increase dynamic range. Where the resistance of CMOS switch is plotted as a function of the input voltage figure 9, In this figure, the p-channel M10 and n-channel M9 devices are sized in such a way that they have an equivalent resistance to identical terminal conditions.

The peak behavior at midrange (near VDD/2), is due the parallel combination of the two devices M9 and M10. In the right n-channel M9 dominating when E is low, and in the left p-channel M10 dominating when E is high (near VDD).

Figure 10 shows a typical variation of the gain and phase versus frequency, with Cc =0.6 pF, Cp=1 pF.

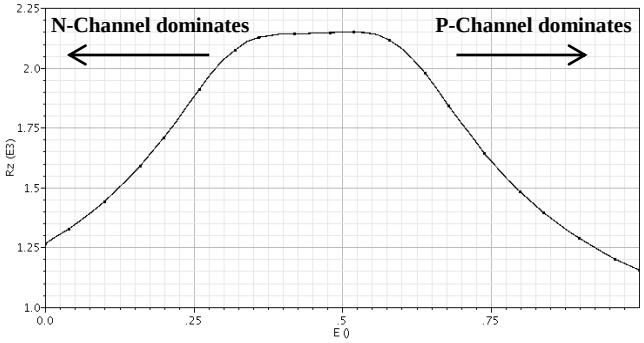

Figure 9. Rz of figure 7, as a Function of E

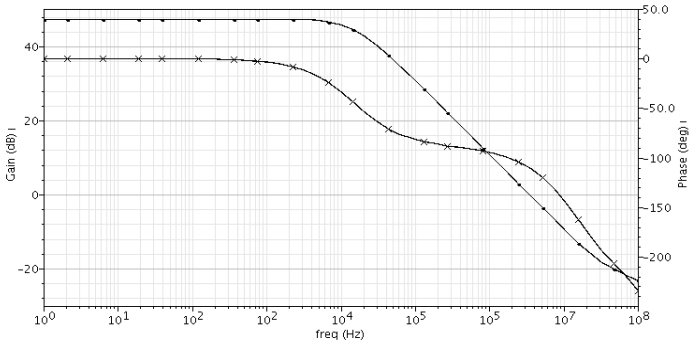

Figure. 10 Shows a Typical Variation of the Gain and Phase versus Frequency

5.3. Common Mode Rejection Ratio CMRR

Due to the large amount of 60-Hz human in bio-potential measurements, common-mode rejection is as important as low-noise operation. CMRR is defined as the ratio of the voltage gain for a differential-mode input signal to the voltage gain for a common-mode input signal, and can be stated as [22], Therefore, measuring the dc CMRR involves determining the change in the offset voltage due to any change in the applied common-mode voltage. But, power supply voltage variation may affect the output as well as the offset voltage. In order to ensure that the measured change in the offset voltage is only due to a change in common-mode input voltage, the output voltage of the Two-stage operational amplifier is maintained at a fixed voltage for the complete test sequence.

We simulate the complete circuit in single power supply for CMRR. The results of CMRR are up to 130dB as shown in Figure 11.

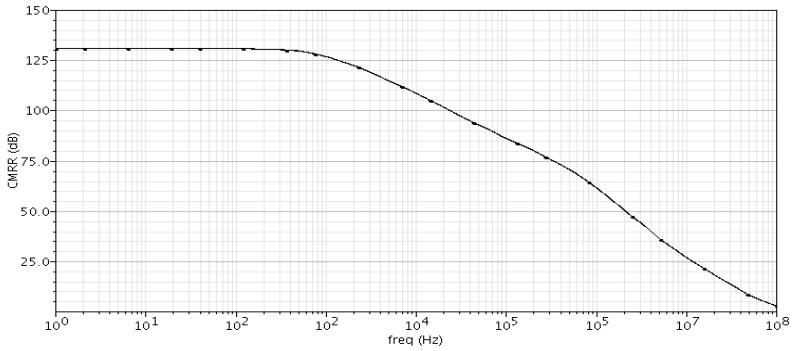

Figure 11. Show a Variation of the CMRR versus Frequency

5.4. Noise

The input stage dominates the noise of the op amp. PMOS devices offer lower flicker noise which is advantageous in our op amp design. Also, the noise component of the load devices is scaled by the ratio of their transconductance to that of the input pair devices. So, the transconductance of the input differential pair needs to be larger than that of the load pair in order to ensure low input-referred noise. There exists a trade-off between noise and the output swing of the stage. Generally, the overdrive voltage of the current loads is minimized to realize a wide output swing, but for a fixed current bias this increases the transconductance (due to increased W) and thereby results in a larger input-referred noise.

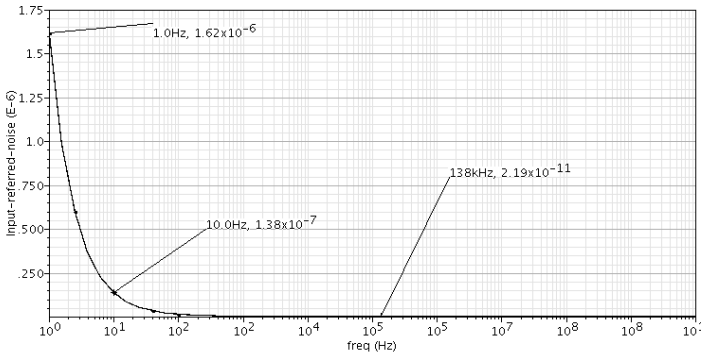

Figure 12. Simulated Input-refred Noise Spectrum

The simulation results of the input referred noise spectrum is depicted in figure 12, flicker noise below 100Hz is clearly visible, it achives input referred noise density of $138nV\sqrt{Hz}$ at 10Hz.

This a standard two-stage 11-transistor amplifier Figure 4 with miller compensation and zero-nulling active resistor Rz=(Rn//Rp). All the devices operate in saturation region except the transistors M9 and M10 operate in the linear region. The input differential stage draws 1uA , while the output stage current is 1.1uA. This results in a total current consumption of 2.1uA plus the current reference Iref=0.5uA , *i.e.*, a 2.6 uW power consumption from single 1V supply.

Figure 13 shows the amplified ECG (Vout) signals, note the original ECG is only 1.5mV in its peak-to-peak magnitude.

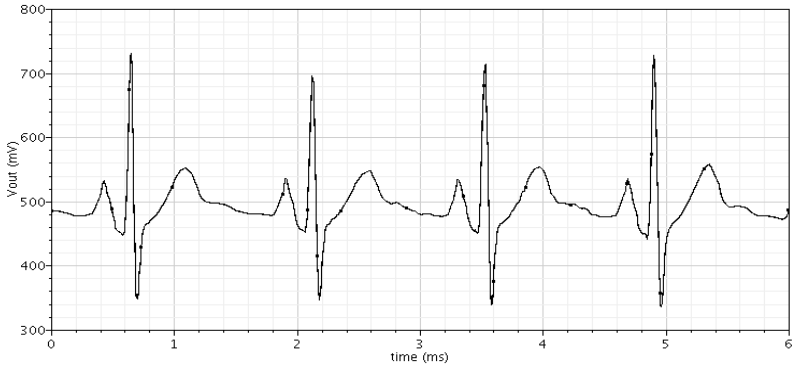

Figure 13. Simulated Results of the Amplified ECG (Vout) Signals

The overall performance summary of the complete circuit two-stage operational amplifier for biomedical applications is given in Table 3.

Table 3. Simulation Results of Schematic Two-stage Amplifier

Process	90nm CMOS
Power supply	1V
Power dissipation	2.6uW
CMRR	131 dB
Bandwidth	15.3kHz
PSRR+	70.7 dB
Ad	55.1 dB
Input offset voltage (Vos)	6.42um
PM	69.46
Input-referred-noise at 10 Hz	$138nV\sqrt{Hz}$

6. Conclusion

In this paper, we present a Two-stage operational amplifier topology for low voltage and low power, ECG Monitoring System applications, This two-stage amplifier with Miller compensation can be used in low power, low voltage High CMRR and PSRR applications such Biomedical instrument and a small battery operated devices. The circuit has been designed in a SPECTRE using 0.90um CMOS technology.

To reduce the noise of the amplifier, we used the P-channel input devices with N-channel load, because it's flicker noise is less than that the N-channel input devices with P-channel load.

We have described an ECG amplifier with low input-referred noise, 131-dB CMRR, less than 3uW of power consumption, and good cardiac signal fidelity.

Proposed two-stage operational amplifier with Miller compensation (Cc) and nulling active resistor (Rz), is well suited to biomedical systems such as cardiac pacemaker, electrocardiogram (ECG) where low-power consumption is of primary concern.

It seems that the input-referred-noise not minimized well, we can reducing flicker noise by using techniques, such as auto-zero-technique, or chopper-stabilization technique.

References

[1] T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schuster and H.N.Yu, "1um MOSFET VLSI technology, Part IV-Hot-electron design constraints", IEEE Trans.Electron.Devices, vol. 26,**(1979)**, pp. 346-353.
[2] M.F.Li, Uday Dasgupta, X. W. Zhang and Yong Ching Lim, "A low-Voltage CMOS OTA with Rail-to-Rail Differential Input Range", IEEE Transactions on circuits and systems, **(2000)** January, vol 47, pp.1-8.
[3] M. Swan, K. Arabi and B. Provost, "Implantable volume monitor and miniaturized simulator dedicated to bladder control", Artificial Organs, vol. 21, no. 3, **(1997)**, pp. 219-222.
[4] R. Stein, B. Charles, D. Davis, L. Jhamandas, J. A. Mannard and T. R. Nichols, "Principles underlying new methods for chronic neural recording", Can. J. Of Neuro.SCI., **(1975)**, pp. 235-244.
[5] D. Popovic, B. Stein, R. B. Jovanovic, K. L. Dai, A. R. Kostovand and W.W. Armstrong, "Sensory nerve recording for closed-loop control to restore motor function", IEEE Trans. Biomed.Eng, vol. 40, no. 10, **(1993)**, pp. 1024-1031.
[6] Y. Hu. and M. Sawan, "CMOS Front-end Amplifier Dedicated to Monitor Very low Amplitude Signal from Imlantable Sensors",Kluwer Academic Publishers, vol. 33, **(2002)**, pp. 29-41.
[7] W.-S. Wang, Z.-C. Wu, H.-T. Huang and C.-H. Luo, "Low Power Instrumental Amplifier for Portable ECG", IEEE Circuits and Systems International Conference, **(2009)**, pp. 1-4.
[8] C.-T. Ma, P.-I. Mak, M.-I. Vai, P. Mak, S.-H. Pun, W. Feng and R.P. Martins, "A 90nm CMOS Bio-Potential Signal Readout Front-End with Improved Powerline Interference Rejection", IEEECircuits and Systems, **(2009)**, pp. 665-668.
[9] C.-C. Huang, S.-H. Hung and J.-F. Chung, "Front-End Amplifier of low-Noise and Tunable B/W Gain for Portable Biomedical Signal Acquidition", IEEE Circuits and Systems, **(2008)**, pp. 2717 – 2720.

[10] D.Yates, E.Lopez-Morillo and R.G.Carvajal, "A Low-Voltage Low-Power Front-End for wearable EEG Systems", Conference of the IEEE EMBS, **(2007)**.
[11] L.Lentola, A. Mozzi, A. Neviani, A. Baschirotto, "A 1uA Front-End for Pacemaker Atrial Sensing Channels",IEEE , **(2009)**.
[12] C. Bronskowski and D. Schroeder, "An ultra low–noise CMOS Operational Amplifier with programmable Noise-Power Trade-off ", IEEESolid-State Circuits Conference, **(2006)**, pp. 368 - 371
[13] J.G. Webster, "Medical instrumentation : Application and design", 3rd ed, John Wiley & sons Inc,**(1998)**.
[14] H.-C. Chow and B.-S. Tang, "A high Performance Current-mode Instrumentation Amplifier For Biomedical applications", 2nd International Conference on Signal Processing Systems, **(2010)**.
[15] C. Ken and L. Xiaoying, "A Zigbee Based Mesh Network for ECG Monitoring System", Bioinformatics and Biomedical Engineering (iCBBE), **(2010)**, pp.1-4.
[16] Y.F. Low, I. B. Mustaffa, N. B. Mohd Saad and A. H. Bin Hamidon, "Development of PC-Based ECG Monitoring System", IEEE Research and Development, 4th Student Conference , **(2006)**, pp.66-69.
[17] PhysioBank, physiologic signal archives for biomedical research, http://www.physionet.org/physiobank/
[18] The MIT-BIH Arrhythmia Database, http:// physionet.org/physiobank/database/mitdb/
[19] The MIT-BIH Compression Test Database, http:// www.physionet.org/physiobank/database/cdb/
[20] R.L. Geiger, P.E. Allen and N.R. Strader, "*VLSI Design Techniques for Analog and Digital Circuits*", McGraw-Hill, **(1990)**.
[21] P.E. Allen and D.R Holberg, "CMOS Analog Circuit Design", Second Edition, Oxford University Press, **(2002)**.
[22] E. J. Kennedy, "Operational Amplifier Circuits, Theory and Applications", Holt, Rinehart and Winston, Inc, New York, **(1988)**.

