International Journal of Bio-Science and Bio-Technology
Vol.6, No.5 (2014), pp.203-214
http://dx.doi.org/10.14257/ijbsbt.2014.6.5.21

Design of 128x8 Pixel Array Fingerprint Sensor with a Capacitive-Sensing Circuit Technique for Image Enhancement

Seung Min Jung

School of Information and Telecommunication, Hanshin University, Osan, Korea
jasmin@hs.ac.kr

Abstract

This paper proposes 128x8 array swipe type fingerprint sensor with a capacitive-sensing technique for image enhancement. The circuit of one pixel includes a pixel level charge-sharing and charge pump to replace an ADC. The circuit also adopts the circuit technique that improves quality of dry finger image captured with capacitive fingerprint sensor LSIs. The proper operation is validated by HSPICE for one-pixel and RTL simulation including logic synthesis for a full chip design on condition of 0.35μm typical CMOS process and 3.3V power. The layout is performed by full custom flow for one-pixel and auto P&R for a full chip. The area of a full chip is 0.161mm^2 (9013μm x 1781μm) and the gate count is 303,329. The area of one-pixel is 58 x 58 μm^2. Pitch is 60 μm and image resolution is 423dpi.

Keywords: *Dry finger, Fingerprint, Sensor, Charge pump, ADC, HDL*

1. Introduction

CMOS processes have been used to produce fingerprint sensor prototypes. Most of them rely on capacitive coupling between the finger and matrix of small metal plates to detect ridges and valleys on the finger surface. Each plate forms a pixel of the resulting image and requires circuitry to measure the capacitance using either DC or AC signals [1-2].

The finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode as shown in Figure 1. One of the most important performances of a capacitive sensor is the sensitivity capability since the detected capacitance is very small of the order of femto-farads. When the finger is placed on the sensor, the electrical charge is extremely weak building a pattern between the finger's ridges or valleys and the sensor's plates. Using these charges the sensor measures the capacitance pattern across the surface. The measured values are digitized by the sensor then sent to the microprocessor. The surface of a capacitive sensor is a neat array of plates, able to measure the capacitance between these plates and the fingerprint contour. The comparator discriminates a ridge and valley by reference voltage. A reference voltage compares the voltage from the sensor and fingerprint's ridge and valley to create binary image. We need a gray scale fingerprint image for more accurate processing of a fingerprint algorithm. Some circuits have been designed to get a gray scale image in semiconductor fingerprint sensor [3]. But these results need a complex module such as digital-to-analog converter (DAC) and large scale layout. This paper adopts the scheme of a gray scale fingerprint image of pixel level for high-accuracy capacitive sensor chip [4].

A sensor for biometrics will be used by various users that have different conditions for sensing [5-7]. The quality of images captured by a capacitive fingerprint senor LSI depends on the finger-surface condition, as shown in Figure 2. The image quality for a dry finger is poor compared to that for a normal finger. The degradation of the image quality is caused by

ISSN: 2233-7849 IJBSBT

the finger surface resistance when the finger is dry, and this is a serious issue for fingerprint identification. To solve this problem, we adopt a capacitive-sensing circuit technique for capturing the clear fingerprint image without the influence of finger surface resistance [3].

In this paper, we propose novel combinational circuit with the sensing scheme for capturing the pixel level gray scale images using charge pump circuit and a circuit technique that improves quality of dry finger image captured from LSIs in Section 2.1 and 2.2. This paper proposes swipe type 128x8 array fingerprint sensor with a capacitive-sensing technique for image enhancement. The concept and design result of the proposed sensing scheme is described in Section 2.3.

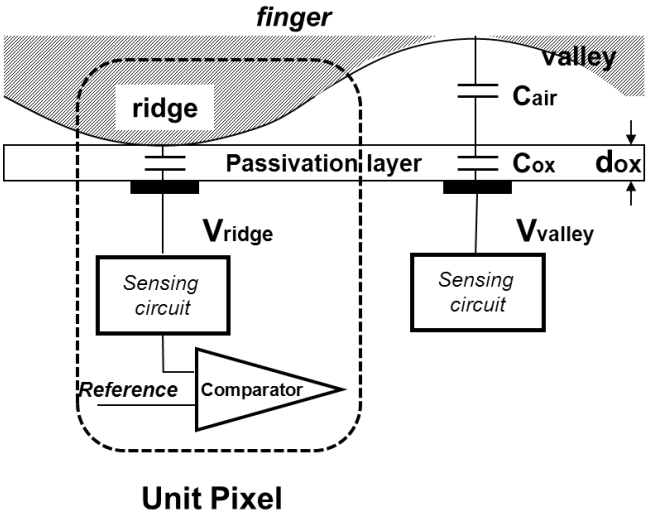

Figure 1. Typical Binary Scale Capacitive Fingerprint Sensing Scheme

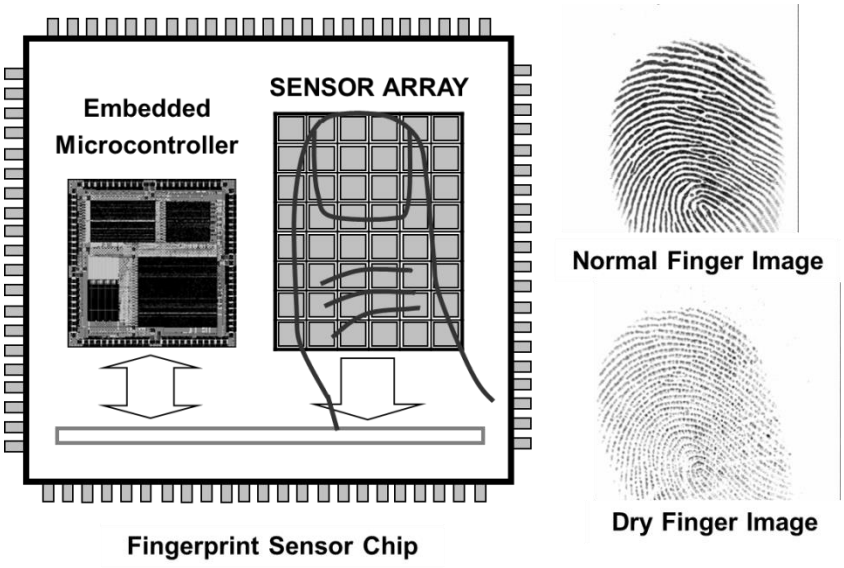

Figure 2. Capacitive Fingerprint Sensor LSI and Captured Image, Whose Quality Depends on the Condition of the Finger Surface

2. Proposed Sensing Scheme

2.1. Sensing Cell with a Charge Pump Circuit

Figure 3 shows the proposed active capacitive charge-sharing sensing scheme and Figure 4 is timing diagram. The capacitance of Cf is at its maximum value when a ridge has contact with the passivation layer. As the distance between the chip surface and the finger's skin increases, the capacitance becomes smaller. In Figure 3, BUFFER is a unit-gain buffer and PCH means precharge signal. When PCH is high, the operation is in the precharge phase. The node N1 and M3 of Cp3 are precharged to VDD, and node Cp2 is discharged to GND. In this phase, no charge is accumulated in Cp3 because the two electrodes have the same potential. In Cp1 and Cf, the amount of charge stored is Cp1•VDD and Cf•VDD. At the beginning of the evaluation phase, the charges are redistributed between the nodes. The BUFFER is enabled as a unit-gain buffer in this phase. The BUFFER tracks the voltage change of the node N1, which makes the potential of Cp3 to zero. Usually, because Cp1 and Cp2 are the parasitic metal routing capacitances, they are much smaller than Cp3. Therefore, the adoption of BUFFER is an effective method to remove the influence of Cp3. In the evaluation phase, the VAC is driving pulse for applying an electrical charge to the finger skin directly. The charge is collected in Cf between finger skin and sensor electrode (M4) by VAC. The amount of charge is various between a ridge and valley. Therefore, V(N1)p_p which is peak to peak voltage of node N1, is larger at a ridge than valley as shown in Figure 4. This paper applies a charge pump circuit for reference voltage generation of comparator as shown in Figure 3. As shown in Figure 5, the output voltage of a charge-pump circuit gradually increases due to non-overlapping two clock signals. One stage is comprised of one diode and actual coupling capacitor. As an effect of diode, the voltage is transferred to only one direction, to show an overall gradual output voltage increase effect. This increased voltage is applied as a comparator's reference voltage. The comparator compares the reference and the sensor voltage then, decides whether the image is a ridge or valley.

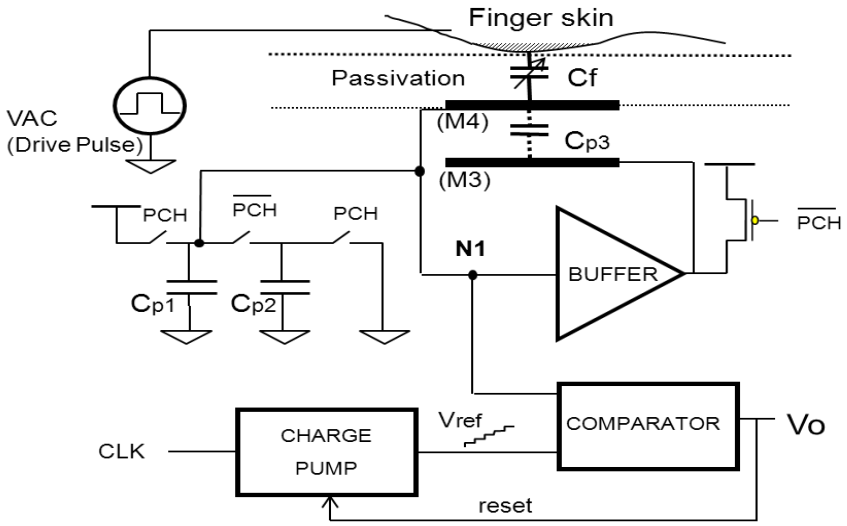

Figure 3. Proposed Active Capacitive Sensing Circuit

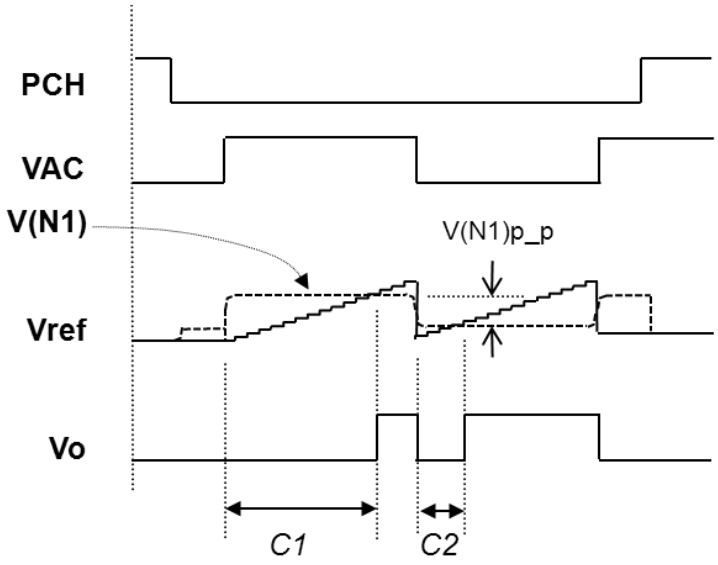

Figure 4. Timing Diagram

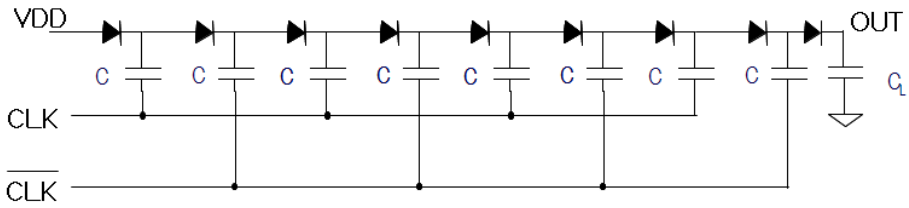

Figure 5. Dickson Charge Pump Model

This paper proposes the operating algorithm for 16-level gray scale image without ADC using a charge pump. At the beginning of VAC rising, the charge pump circuit receives clock CLK from microcontroller to increase comparator's reference voltage. The comparator compares the fingerprint sensing voltage of node N1 and reference voltage of charge pump circuit. It then saves the number of clock, at the changing point, where logic is changed from 0 to 1, in a memory. The number of clock is C1 at high driving pulse as shown in Figure 4. The charge pump is reset at the beginning of VAC falling. The comparator compares the fingerprint detection voltage created by the sensor and charge pump circuit output, reference voltage again. It also saves the number of clock, at the point where logic is changed from 0 to 1. The number of clock is C2 at low driving pulse as shown in Figure 3. Finally, microcontroller subtracts each pixel's value of C2 from C1, which is a corrected image. The final clock count value is 16-level gray scale image and it also is saved in a memory.

Figure 6 shows the implementation of the proposed active capacitive-sensing circuit on Cadence environment and Figure 7 shows 6-stage charge pump circuit. The proper operation can be seen by HSPICE simulation of one pixel on condition of 0.35μm typical CMOS model parameter and 3.3V power supply in Fig 8, 9 and 10. By effective removing of parasitic capacitance Cp3 using unit gain buffer, the peak to peak voltage of ridge is 1381mV and the value of valley is 80mV. The peak to peak swing time is larger at ridge than valley as shown in Fig 9 and 10. Thereby, the comparator easily

discriminates a ridge and valley and microcontroller subtracts each pixel's value of C1 from C2, which is gray image value. The final number of clock count is a 16-level gray scale image, and it also is saved in a memory.

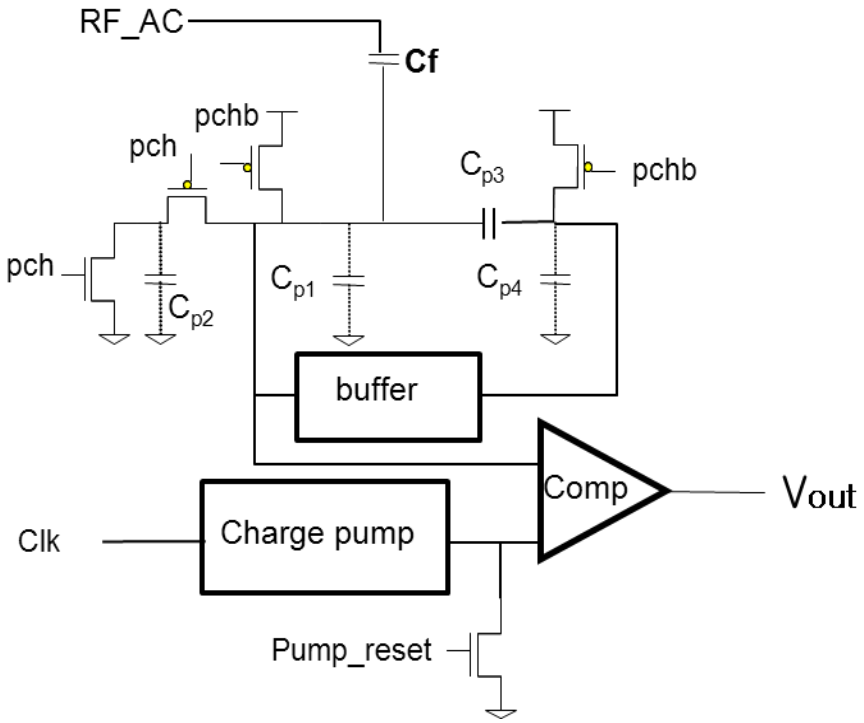

Figure 6. Active Charge-sensing Circuit Implementation

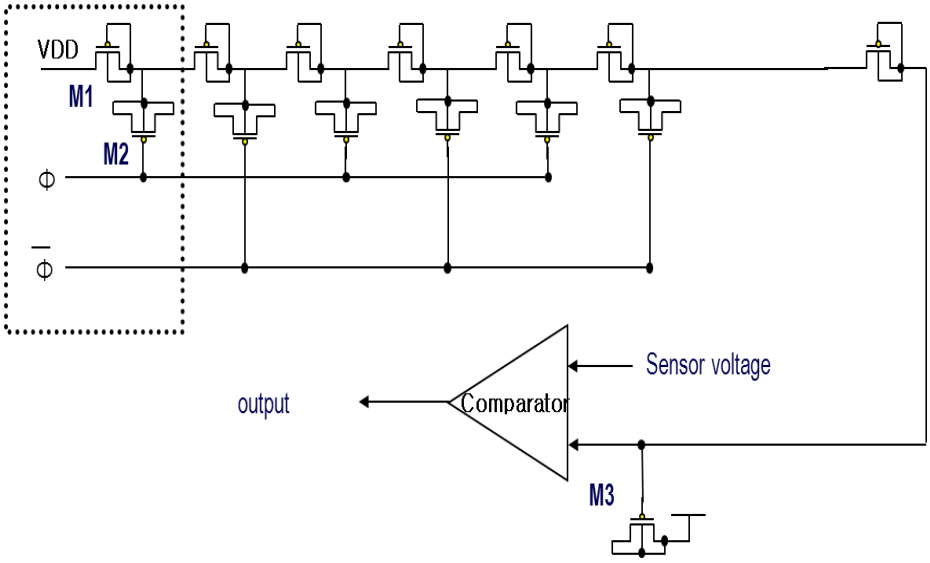

Figure 7. 6-stage Charge Pump Circuit

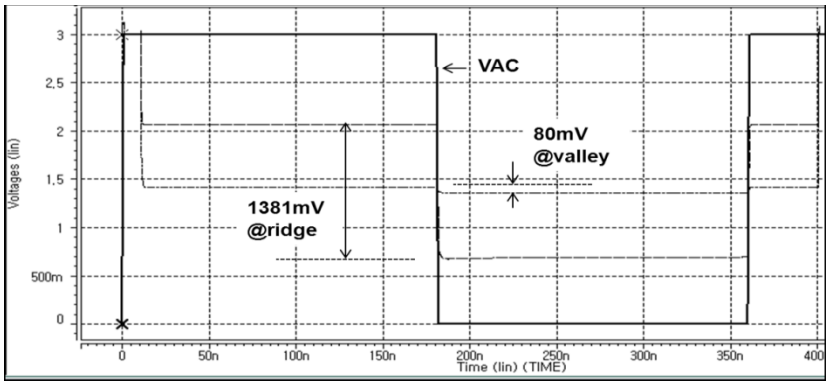

Figure 8. Peak to Peak Voltage of Sensing Output at Ridge and Valley

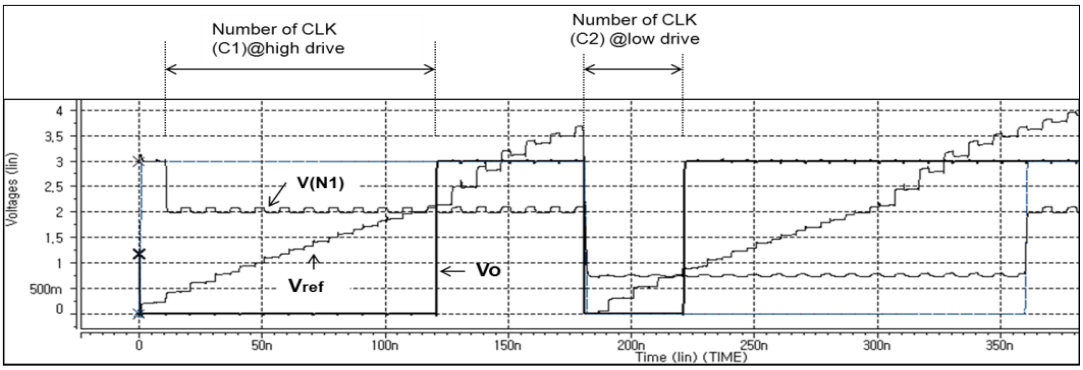

Figure 9. Comparator Output at Ridge

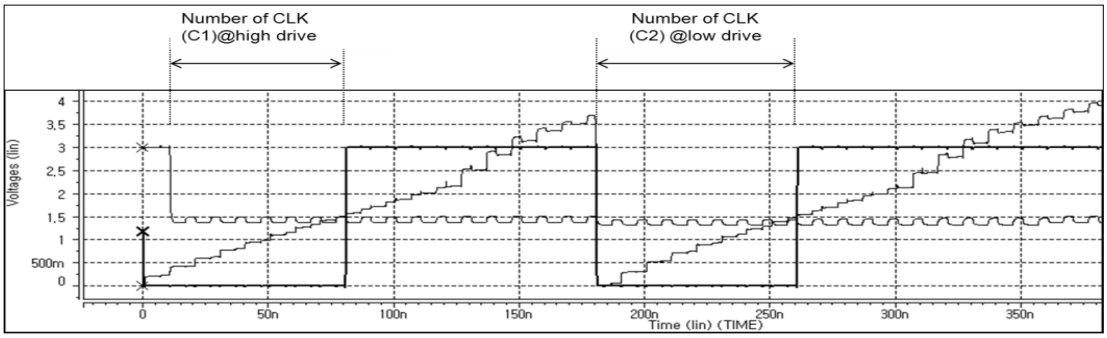

Figure 10. Comparator Output at Valley

2.2. Sensing Cell for Dry Finger Image

In fingerprint sensing, the image quality degrades when the finger is dry. The reason for the degradation is explained using an equivalent circuit model of the finger with the sensing circuit as shown in Figure 11. The finger model is given by the series connection of the sensed capacitance and the resistance of the finger surface Rf. Skin resistivity varies from one person to another and depends also on skin humidity and mechanical pressure applied on the sensor. A skin resistivity varies from 1 MΩ to 10 MΩ in dry conditions. A resistivity of 100 KΩ has been measured in the case of humid skin[3]. The detection of Cf is based on the voltage change in the sensor plate, $\triangle Vs$,

caused by the current source pulling out the charge △Qs from it after the pre-charge operation. When the current source pulls out △Qs, charge △Qr that flows through resistance Rf induces a voltage drop in node N1. This influences the voltage of the sensor plate Vs used for the detection of Cf. Figure 12 shows simulation results of the sensing voltage difference △Vs on (a) wet fingerand (b) dry fnger at 0.35μm CMOS process. The detection voltage difference between of a ridge and valley is dramatically reduced on a dry finger by a voltage drop in node N1 caused by skin resistance Rf.

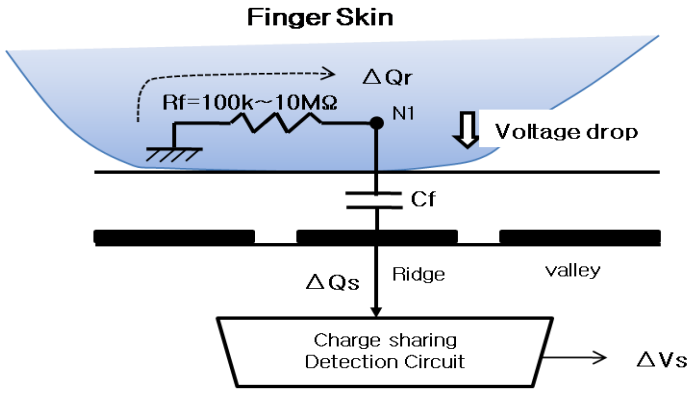

Figure 11. Fingerprint Equivalent Circuit Model with Skin Resistance

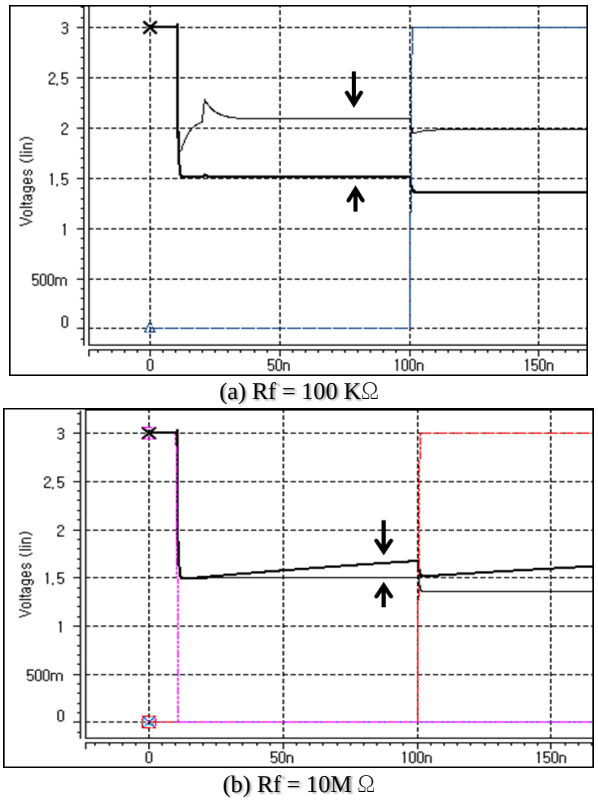

Figure 12. Sensing Voltage Difference △Vs on (a) Wet Finger and (b) Dry Finger (0.35μm CMOS Process)

The modified circuit technique for capacitive sensing suppresses the influence due to the voltage drop in Rf and enhances the contrast between the ridges and valleys. As illustrated in Figure 13, the technique is based on the concept of voltage drop suppression. An enhancement circuit consisting of an enhancement plate is positioned next to the sensor plate and a voltage control circuit is connected to the enhancement plate. The principle of the technique is explained by considering the equivalent circuit model with the enhancement plate. In general, it is known that the finger skin has two layers - the outer skin and inner skin—and the impedance of the outer skin is higher. This circuit model is based on the assumption that the layer of the outer skin acts as an insulator and that of the inner skin acts as a conductor. Under this assumption, the capacitance formed in the enhancement plate Cc is connected to node Nf in the equivalent circuit. The voltage control circuit generates charge △Qc using capacitance Cc. The current generated due to △Qc, which has the inverse direction of the current due to △Qs, changes the current direction of △Qr in Rf, thereby preventing the voltage drop, In this way, the voltage control circuit raises the potential of the finger through the capacitance of the enhancement plate [3]. This enhances the sensitivity of the capacitive sensing when the finger is dry. The concept of generating the inverse current in finger surface resistance is valid for other sensors suffering degradation of sensitivity for sensed capacitance due to series-connected resistance. To implement the circuit technique that enhances the sensitivity using the voltage drop suppression, we used the sensing circuit shown in Figure 13. The enhancement circuit has a voltage control circuit that generates a pulse signal using a buffer gate. The sensing signal that starts a sensing operation is input into the current source of the sensing circuit and the voltage control circuit. Figure 14 shows simulation results of the sensing voltage difference △Vs on dry finger at 0.35μm CMOS process. The detection voltage difference between of a ridge and valley is almost same with the value of a wet or normal finger skin even though at a dry finger (Rf=10M Ω).

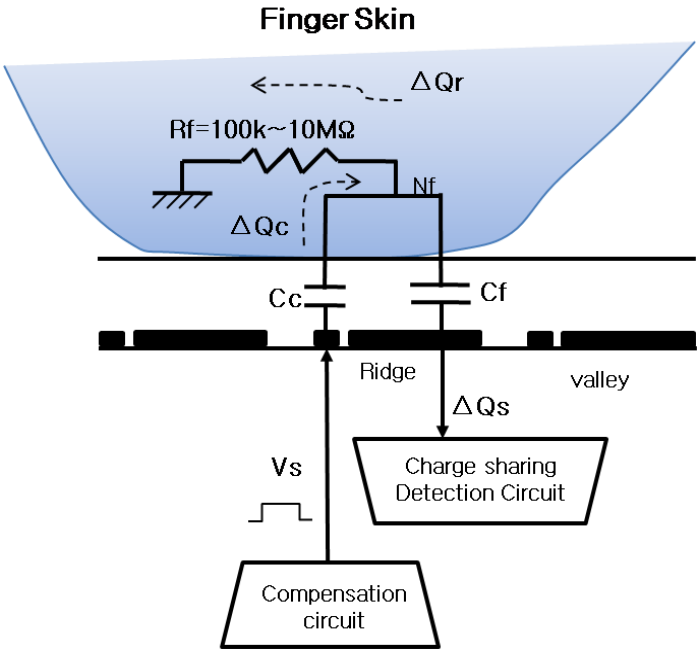

Figure 13. Configuration of Sensing Circuit with the Enhancement Circuit

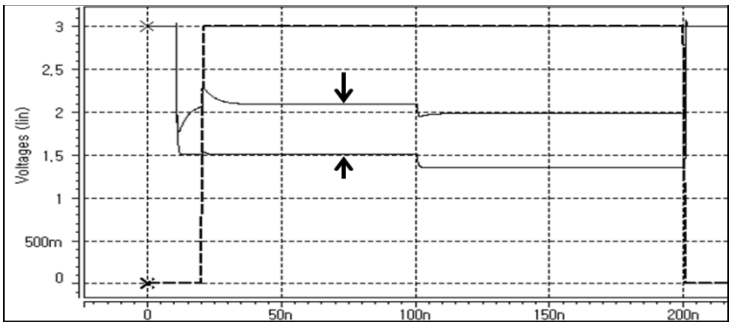

Figure 14. Sensing Voltage Difference △Vs on a Dry Finger (Rf=10M Ω, 0.35μm CMOS Process)

2.3. Implementation of Proposed Sensing Technique

Figure 15 shows the one-pixel circuit of proposed sensing technique. The circuit is composed with typical charge sharing sensing circuit block, charge pump block to replace an ADC, and compensation circuit with buffer gate that improves quality of dry finger image captured with capacitive fingerprint sensor LSIs. The plate of new sensor is divided into two plates. Cc is compensation capacitor for a dry finger image and coupled with a pulse signal for reducing voltage drop by dry skin resistance Rf. Figure 16 shows a layout of one pixel and the area is 58μm x 58μm. The image resolution is 423dpi. Figure 17 shows a chip block diagram of the proposed swipe type fingerprint sensor with 128x8 pixel array. Figure 18 shows the design flow of chip implementation. Figure 19 shows 128x8 pixel array chip layout and the area is 9013μm x 1781μm on 0.35μm standard CMOS process. The gate count is 303,329. The layout of 128x8 array core cell is performed by full custom design method and the full chip is performed by auto placement and routing of cell based design method. The fabrication is future work.

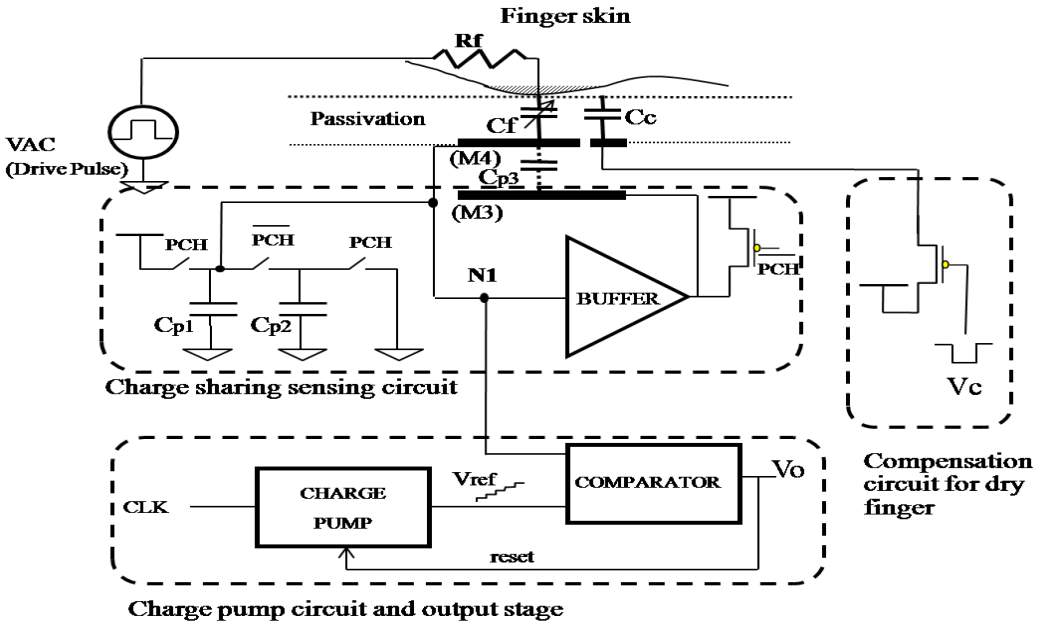

Figure 15. One Pixel Circuit of Proposed Sensing Technique

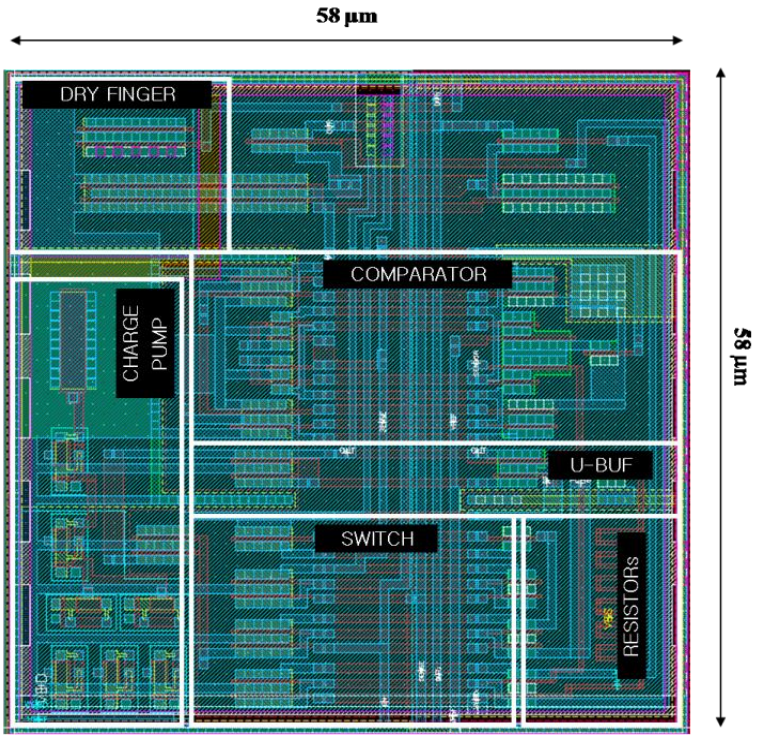

Figure 16. One Pixel Layout (58 μm x 58 μm @0.35μm CMOS Process)

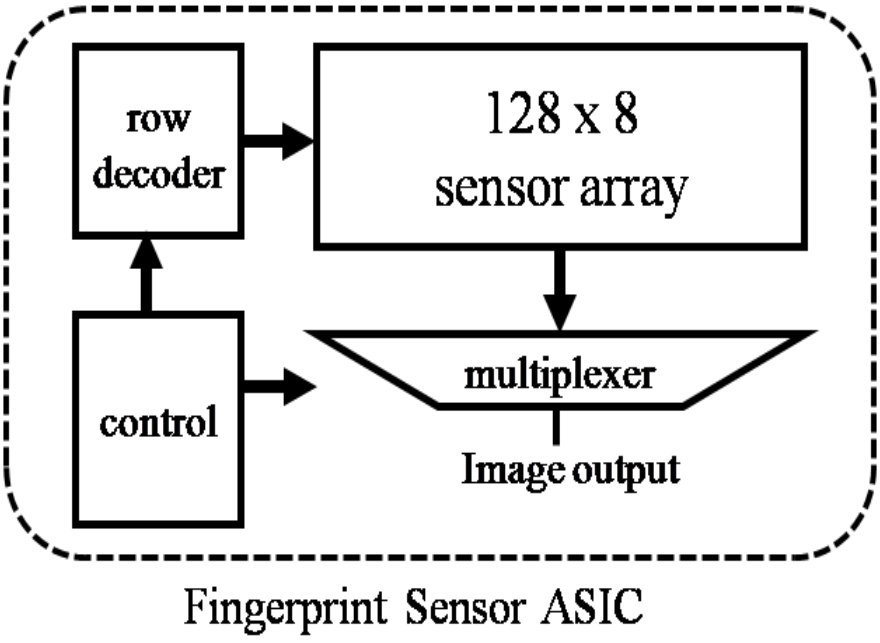

Figure 17. Chip Architecture

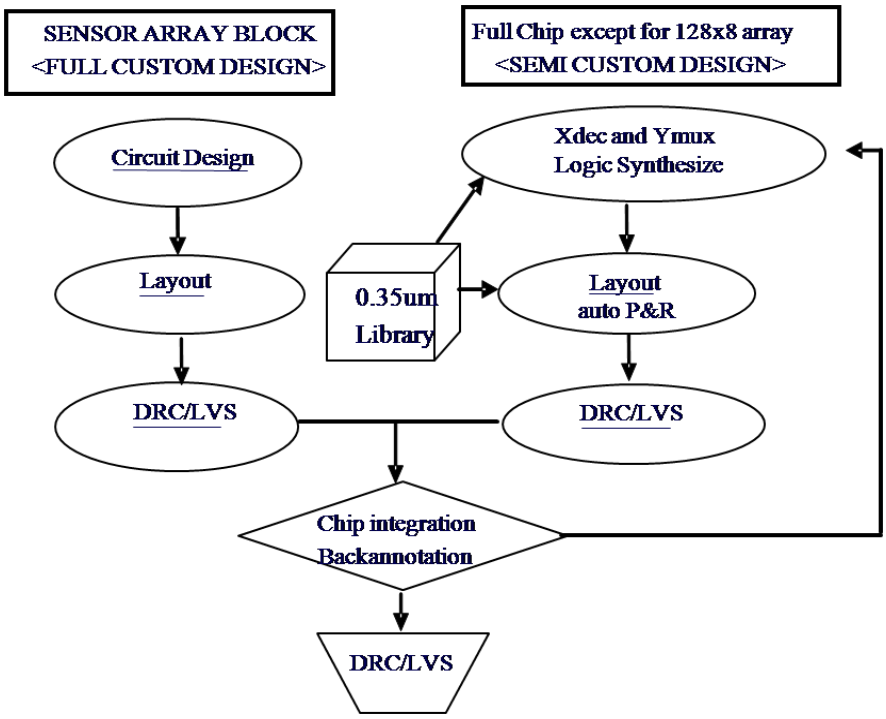

Figure 18. Chip Architecture

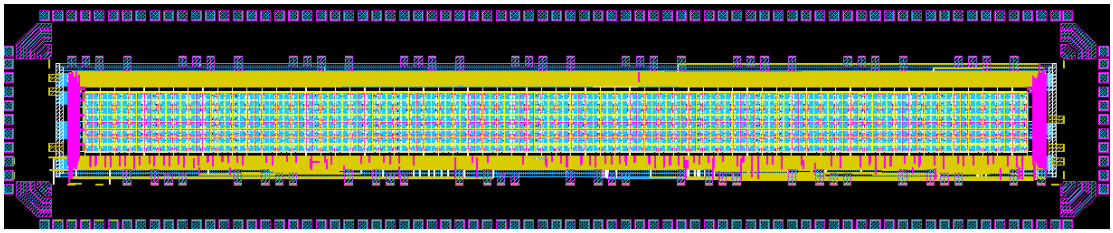

Figure 19. 128x8 Pixel Array Chip Layout (9013 μm x 1781 μm @0.35μm CMOS Process)

3. Conclusion

This paper proposes 128x8 array swipe type fingerprint sensor with a capacitive-sensing technique for image enhancement. We propose novel combinational circuit with the sensing scheme for capturing the pixel level gray scale images using charge pump circuit and circuit technique that improves quality of dry finger image captured from LSIs. The circuit includes a pixel level charge-sharing and charge pump to replace an ADC. The charge pump circuit is adopted for reference voltage generation of comparator. The output voltage of a charge-pump circuit gradually increases due to non-overlapping two clock signals. The comparator compares the reference and the sensor voltage then, decides whether the image is a ridge or valley. This paper proposes the operating algorithm for 16-level gray scale image without ADC using the charge pump. A microcontroller subtracts each pixel's value of ridge clock number from a valley, which is a corrected image. The final clock count value is 16-level gray scale image and it also is saved in a memory. The circuit also adopts the circuit technique that improves quality of dry finger image captured with capacitive fingerprint sensor

LSIs. The modified circuit technique for capacitive sensing suppresses the influence due to the voltage drop by a finger skin resistance and enhances the contrast between the ridges and valleys. The proper operation is validated by HSPICE for one-pixel and Verilog-HDL for a full chip simulation with condition of 0.35μm typical CMOS process and 3.3V power. Full chip logic is synthesized and integrated with 128x8 array sensor core. The layout is performed by full custom flow for one-pixel and auto P&R for a full chip. The area of a full chip is 0.161mm^2 (9013μm x 1781μm) with 164 input and output pads. The gate count is 303,329 and one-pixel is 58 x 58 μm^2 on 0.35μm standard CMOS process. Pitch is 60 μm and image resolution is 423dpi.

Acknowledgements

This work was supported by Hanshin University Research Grant.

References

[1] T. Shimamura, N. Shimoyama, T. Sakata, S. Shigematsu, K. Machida and M. Nakanishi, "Impedance-Sensing Circuit Techniques for Integration of a Fraud Detection Function Into a Capacitive Fingerprint Sensor", IEEE Sensors Journal, vol. 12, no. 5, **(2012)**, pp 1393-1401.
[2] S. M. Jung, J. M. Nam, D. H. Yang and M. K. Lee, "A CMOS Integrated Capacitive Fingerprint Sensor with 32-bit RISC Microcontroller", IEEE Journal of Solid-state Circuit, vol. 40, no. 8, **(2005)**, pp. 1745-1750.
[3] T. Shimamura, H. Morimura, S. Shigematsu, M. Nakanishi and K. Machida, "Capacitive-Sensing Circuit Technique for Image Quality Improvement on Fingerprint Sensor LSIs", IEEE Journal of Solid-state Circuit, vol. 45, no. 5, **(2010)**, pp. 1080-1086.
[4] S. M. Jung, "Active Capacitive-Sensing Circuit Technique for Image Quality Improvement on Fingerprint Sensor", Journal of Next Generation Information Technology (JNIT), vol. 4, no. 3, **(2013)**, pp. 47-53.
[5] J, C. Liu, Y. S. Hsiung and M. Lu, "A CMOS Micromachined Capacitive Sensor Array for Fingerprint Detection", IEEE Journal of Solid-State Circuits, vol. 12, no. 5, **(2012)**, pp. 1004–1010.
[6] L. Li, K. Lv and N. He, "An improved cross-matching algorithm for fingerprint images from multi-type sensors", 2011 4th International Congress on Image and Signal Processing, vol. 3, **(2011)**, pp. 1472–1475.
[7] J. M. Nam, S. M. Jung and M. K. Lee, "Design and implementation of a capacitive fingerprint sensor circuit in CMOS technology", Sensors and Actuators A: Physical, vol. 135, no. 1, **(2007)**, pp. 283-291.

Author

Seung Min Jung received the BS, MS and Ph.D. degrees in electronic engineering from Yonsei University, Seoul, Korea, in 1990, 1992 and 2006. From 1992 to 1997, he was Senior Engineer of the ASIC Division at the SAMSUNG Electronics Co., where he worked on the design of memory compiler. He also worked on the design of mixed signal VLSI. From 1998 to 2006, he joined the faculty of Yongin-Songdam University, Yongin, Korea, where he was assistant professor in the Information and Communication Department. In 2006, he joined the faculty of Hanshin University, Osan, Korea, where he is currently professor in the School of Information and Telecommunication. His research interests include biometric CMOS sensors, SoC design and high-speed interface mixed circuit design. (email: jasmin@hs.ac.kr).

